A CMOS WIRELESS INTERCONNECT SYSTEM FOR MULTIGIGAHERTZ CLOCK DISTRIBUTION

By

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As the clock frequency and chip size of high-performance microprocessors increase, it becomes increasingly difficult to distribute signals across the chip, due to increasing propagation delays and decreasing allowable clock skew. This dissertation presents the design, implementation, and feasibility of a wireless interconnect system for clock distribution. The system consists of transmitters and receivers with integrated antennas communicating via electromagnetic waves at the speed of light. A global clock signal is generated and broadcast by the transmitting antenna. Clock receivers distributed throughout the chip detect the signal using integrated antennas, amplify and divide it down to a local clock frequency, and buffer and distribute these signals to adjacent circuitry.

First, the design and implementation of CMOS receiver circuitry used for wireless interconnects is presented. A design methodology is developed for CMOS low noise amplifiers and demonstrated with a 0.8-μm, 900-MHz amplifier achieving a 1.2-dB noise figure and a 14.5-dB gain. Amplifiers are also demonstrated at 7.4, 14.4, and 23.8 GHz,

using 0.25-, 0.18-, and 0.10-μm technologies, respectively. A design methodology based on injection locking is developed for CMOS frequency dividers, and a programmable divider which limits clock skew is presented. Dividers operating up to 10, 15.8, and 18.8 GHz are demonstrated, implemented in 0.25-, 0.18-, and 0.10-μm technologies, respectively.

Results for the overall wireless interconnect system are then presented. System requirements (gain, matching, noise, linearity) for wireless clock distribution are derived, including specifications for signal-to-noise ratio versus clock jitter, and amplitude mismatch versus clock skew. Wireless interconnect systems are demonstrated for the first time using on-chip antenna pairs, clock receivers, and clock transmitters. The interconnects operate across 3.3 mm at 7.4 GHz, using a 0.25-μm technology, and across 6.8 mm at 15 GHz, using a 0.18-μm technology. Using the 6.8-mm, 15-GHz interconnect, a 25-ps clock skew and 6.6-ps peak jitter have been measured at 1.875 GHz for two receivers separated by ~3 mm. Finally, the wireless interconnect system is analyzed in terms of power dissipation, synchronization, process variation, latency, and area. These results indicate the feasibility of an intra-chip wireless interconnect system using integrated antennas.

CHAPTER 1
INTRODUCTION

1.1 Global Interconnect Challenges

According to the 1999 International Technology Roadmap for Semiconductors (ITRS) [SIA99], at the 0.10 and 0.05-μm technology generations, chip areas for high-performance microprocessors are projected to be approximately 620 and 820 mm^2, respectively. On-chip global clock frequencies are projected to be 2 and 3 GHz, while local clock frequencies are projected to be 3.5 and 10 GHz, respectively. These trends for high-performance microprocessors are shown in Table 1-1. In such integrated circuits (ICs), the delay associated with global interconnects--those which connect functional units across the IC--has become much larger than the delay for a single logic gate (herein termed gate-delay). This is shown in Figure 1-1, which plots the global interconnect delay and gate-delay versus minimum feature size [SIA99, Boh95]. As feature size decreases, gate-delay decreases, illustrating the well-known fact that transistor scaling improves device performance and chip density simultaneously. However, the propagation delay of a voltage wave is approximately equal to $0.35RCl^2$ [Wes92], where l is the length of a wire, and R and C are its resistance- and capacitance-per-unit-length. As the CMOS technology is scaled to smaller feature sizes, both the RC time-constant [Boh95, Tau98] and the chip area (l^2) increase. Therefore, the global interconnect delay increases and quickly begins to dominate the overall system delay.

Table 1-1 Technology Trends of Semiconductor Industry for Microprocessors[+]

Year Technology Node	1999 180nm	2002 130nm	2005 100nm	2008 70nm	2011 50nm
Microprocessor Gate Length (nm)	140	85-90	65	45	30-32
Microprocessor Chip Size (mm^2)	450	~508	622	713	817
Linear Dimension of Chip (mm)	21.2	22.5	24.9	26.7	28.6
Local CLK (MHz)	1,250	2,100	3,500	6,000	10,000
Global CLK (MHz)	1,200	1,600	2,000	2,500	3,000
Metal Layers	7	8	9	9	10
Power Dissipation (W)	90	130	160	170	174
10% Global Skew Requirement (ps)	83	62	50	40	33

[+]Source: 1999 International Technology Roadmap for Semiconductors [SIA99]

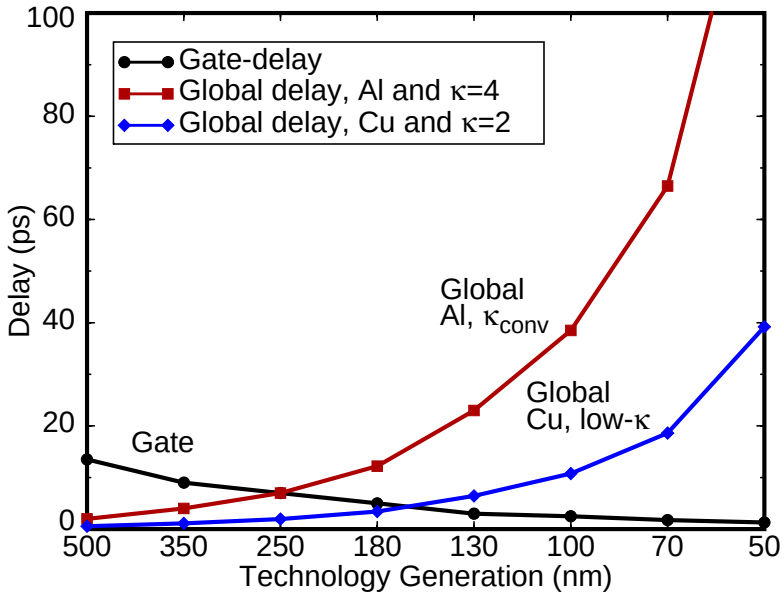


Figure 1-1 Global interconnect delay and gate-delay versus technology generation for aluminum and copper metallization and conventional and low-κ dielectrics.

To offset this problem, copper (Cu) interconnects and low-κ dielectrics have been introduced, decreasing the global propagation delay by a ratio of approximately $\rho_{Cu}\kappa_{low}/\rho_{Al}\kappa_{conv}$, where ρ is the resistivity of copper (aluminum) and κ is the relative dielectric

constant for low-κ (conventional) dielectrics. This corresponds to a downward shift in the global delay plotted in Figure 1-1. Unfortunately, since the delay scales with chip area, despite the addition of copper and low-κ dielectrics, global interconnect delay will continue to increase with succeeding generations of microprocessors. Copper and low-κ dielectrics only extend the lifetime of conventional (i.e., traditional conductor) interconnect systems a few technology generations. In particular, the global delay is still much larger than the gate-delay for the 0.10-μm technology node and beyond.

The global interconnect delay is especially detrimental to global clock signal distribution. Global clock signals need to be distributed across the microprocessor with skews of less than ten percent of the global clock period. With each succeeding generation of microprocessor, the clock frequency increases, decreasing the clock period and thus the skew requirement in absolute time. This is in contrast to chip area and propagation delay, which are both increasing. Hence, techniques are required to equalize the increasingly large delays of each distributed clock signal to even greater accuracies or lower absolute clock skews. Another serious issue with global clock distribution is the dispersion associated with interconnect resistance. A non-zero interconnect resistance causes the harmonics of the clock signal to travel at different velocities through the interconnect, resulting in an increase (i.e., slowing) of the rise and fall times of the signal. As the interconnect length is increased, the rise and fall times increase, and they can ultimately limit the maximum frequency of the signal [Deu98].

Both of the previously stated problems have been somewhat circumvented in the ITRS for 0.13-μm generations and beyond by distributing a lower frequency global clock and allowing functional units to operate off of a higher frequency local clock. However,

referring to Table 1-1, there is an increasing gap between the projected local and global clock signal frequencies, underscoring the shortcomings of current global clock distribution systems. Clearly, advanced interconnect systems capable of distributing high frequency signals with short propagation delays and minimal power dissipation are needed to address these concerns.

1.2 Proposed Interconnect System

1.2.1 Potential Solutions

Potential solutions to address the limitations of conventional global interconnect systems can currently be categorized as follows: (1) further modifying the properties of conductors, such as cooled metal [All00] or superconductive metal, (2) shortening the distance of global interconnects by using three-dimensional structures, or (3) shifting away from synchronous computer architectures towards asynchronous architectures. A final category of solutions requires thinking even more “outside of the box” and entails research of a more fundamental nature as follows: (4) using alternative mediums to distribute signals, such as optical [Mil97] or organic mediums. However, all of the examples just listed require significant development and/or changes to either the semiconductor materials, manufacturing process, or circuit design process. An alternative global interconnect system of the fourth category is to distribute signals at the speed of light using microwaves and antennas, employing a conventional CMOS technology. This system is termed a wireless or radio-frequency (RF) interconnect system [O97, O99, Flo00a].

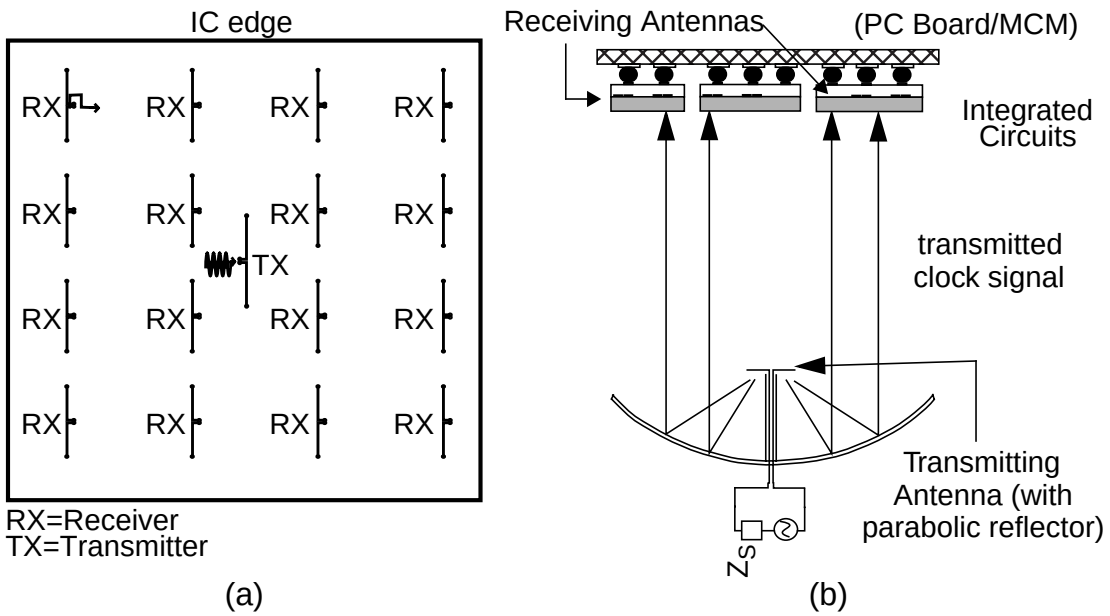


Figure 1-2 Conceptual system illustrations of (a) intra-chip and (b) inter-chip wireless interconnect systems for clock signal distribution.

1.2.2 Description of Wireless Interconnect System

The wireless interconnect system consists of integrated receivers and transmitters with on-chip antennas which communicate across a single chip or between multiple chips via electromagnetic waves. Wireless interconnects can be used for both data and clock signals. However, for wireless data, a modulation scheme is required, while for a wireless clock, only a single tone is required. Therefore, wireless clock distribution is a natural first step for evaluating the potential of wireless interconnects in general as well as for developing the key components of a wireless interconnect system. For these reasons, wireless clock distribution is studied in this work.

A conceptual illustration of a single-chip or intra-chip wireless interconnect system for clock distribution is shown in Figure 1-2(a). An approximately 20-GHz signal is generated on-chip and applied to an integrated transmitting antenna which is located at one part of the IC. Clock receivers distributed throughout the IC detect the transmitted

20-GHz signal using integrated antennas, and then amplify and synchronously divide it down to a ~2.5-GHz local clock frequency. These local clock signals are then buffered and distributed to adjacent circuitry. Figure 1-2(b) shows an illustration of a multi-chip or inter-chip wireless clock distribution system. Here the transmitter is located off-chip, utilizing an external antenna, potentially with a reflector. Integrated circuits located on either a board or a multi-chip module each have integrated receivers which detect the transmitted global clock signal and generate synchronized local clock signals.

1.2.3 Clock Receiver and Transmitter Architectures

Figure 1-3(a) shows a simplified block diagram for an integrated clock transmitter. The ~20-GHz signal is generated using a voltage-controlled oscillator (VCO). The signal

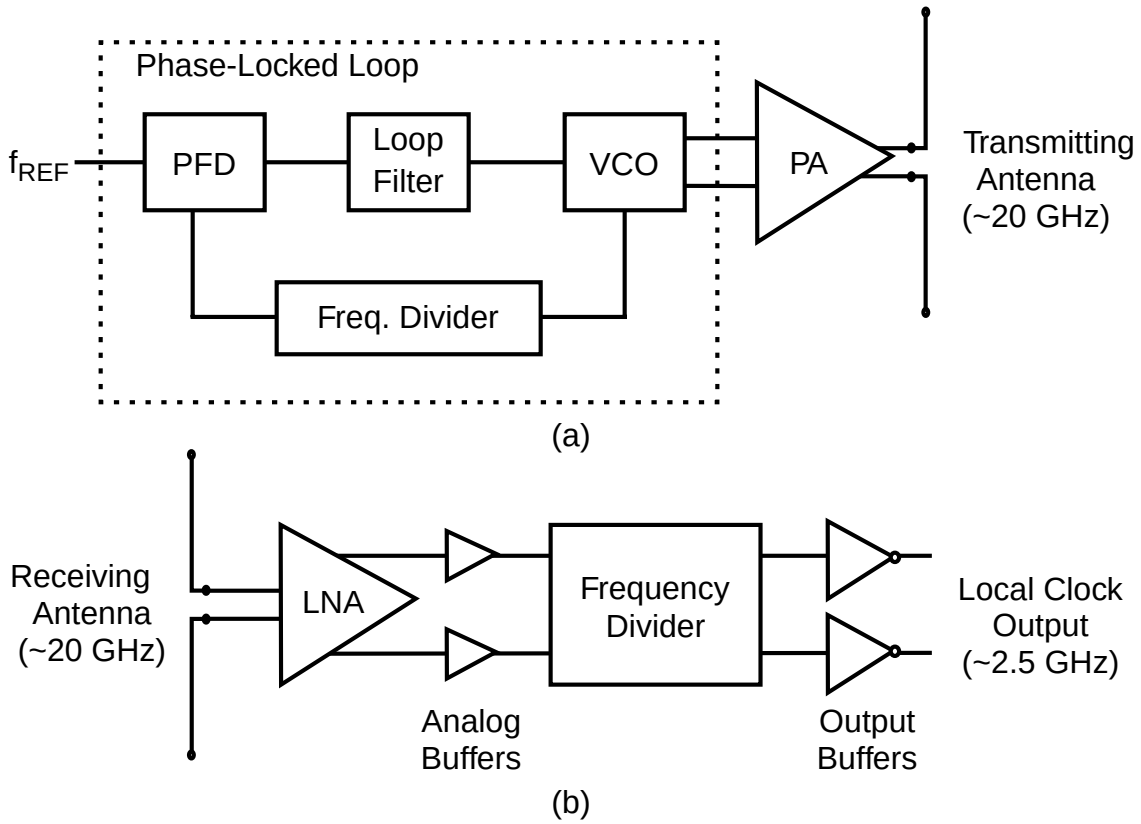


Figure 1-3 Block diagrams of (a) integrated clock transmitter and (b) integrated clock receiver.

from the VCO is then amplified using a power amplifier (PA), and fed to the transmitting antenna. The VCO is phase-locked to an external reference using a phase-locked loop (PLL), providing frequency stability. The PLL consists of a phase-frequency detector (PFD), a loop filter, the VCO, and a frequency divider.

Figure 1-3(b) shows a block diagram for an integrated clock receiver. The global clock signal is detected with a receiving antenna, amplified using a low noise amplifier (LNA), and divided down to the local clock frequency. These local clock signals are then buffered and distributed to adjacent circuits. The amplifier is tuned to the clock transmission frequency to reduce interference and noise. Since the microprocessor is extremely noisy at the local clock frequency and its harmonics, transmitting the global clock at a frequency higher than the local clock frequency provides a level of noise immunity for the system [Meh98]. Also, operating at a higher frequency decreases the required antenna size. The receiver is implemented in a fully differential architecture, which rejects common-mode noise (e.g., substrate noise) [Meh98, Brav00a], obviates the need for a balanced-to-unbalanced conversion between the antenna and the LNA, and provides dual-phase clock signals to the frequency divider.

1.2.4 Potential Benefits

The wireless clock distribution system would address the interconnect needs of the semiconductor industry in providing high-frequency clock signals with short propagation delays. These needs would be met while providing multiple benefits. First, signal propagation occurs at the speed of light, shortening the global interconnect delay without requiring integrated optical components. Second, the global interconnect wires used in conventional clock distribution systems are eliminated, freeing up these metal layers for

other applications. Third, referring to Figure 1-2(b), the inter-chip clock distribution system can provide global clock signals with a small skew to an area much greater than the projected IC size. This is an additional benefit, possibly allowing synchronization of an entire PC board or a multi-chip module (MCM). Fourth, in the wireless system, dispersive effects are minimized since a monotone global clock signal is transmitted. Fifth, another benefit is a more uniformly distributed power load equalizing temperature gradients across the chip. Sixth, by adjusting the division ratio in the receiver, higher frequency local clock signals [SIA99] can be obtained, while maintaining synchronization with a lower frequency system clock. Seventh, an intangible benefit of wireless interconnect systems is the effect they could have on microprocessor or system implementations, potentially allowing paradigm shifts such as drastically increased chip size. Finally, compared to other potential breakthrough interconnect techniques, such as optical, superconductive, or organic, a wireless approach based on silicon seems to be a potential solution which is compatible with the technology trends of the semiconductor industry.

1.2.5 Areas of Research

The main areas of research for wireless clock distribution are as follows: integrating compact power-efficient antenna structures, identifying noise-coupling mechanisms for the wireless clock distribution system and estimating the signal-to-noise ratio that can be achieved on a working microprocessor, implementing the required 20-GHz circuits in a CMOS process consistent with the ITRS, and characterizing a wireless clock distribution system in terms of skew and power consumption and estimating the overall feasibility of the system. The first two items have been discussed in detail in separate research

dissertations [Meh98, Brav00a, Kim00a] and are still being actively pursued, while the last two items are the subject of this dissertation.

1.3 Overview of Dissertation

This dissertation focuses on the implementation of an intra-chip wireless clock distribution system and evaluation of its feasibility, serving as a natural first step for evaluating the potential of both intra- and inter-chip wireless interconnects. This work will emphasize the design and implementation of RF CMOS receiver circuitry, and will evaluate the system feasibility by implementing both single-link (one transmitter/one receiver) and multi-link (one transmitter/multiple receivers) wireless interconnects.

The low noise amplifier (LNA) is the first component in the clock receiver, and through its low noise figure and moderate gain, it approximately sets the signal-to-noise ratio of the entire receiver. Generally, CMOS LNAs have had inferior performance compared to silicon bipolar or gallium-arsenide (GaAs) LNAs. Also, there are very few examples of CMOS LNAs operating above 5.8 GHz. Chapter 2 presents a new design methodology for source-degenerated CMOS LNAs, examining input and output matching, gain, and noise parameters. The effects of substrate resistance, gate-induced noise, and input-matching variations are considered. These methodologies are demonstrated in Chapter 3, where the implementation and measured results of source-degenerated CMOS LNAs operating at 0.9, 8, and 14 GHz, and implemented in 0.8-, 0.25-, and 0.18-μm CMOS technologies are presented. Also, a 23.8-GHz tuned amplifier with a common-gate input implemented in a partially-scaled silicon-on-insulator (SOI) 0.1-μm CMOS technology is presented. These LNAs are intended for use in clock receivers; however, the results are also applicable to standard CMOS receivers.

In the clock receiver, the frequency divider translates the ~20-GHz global clock signal to a ~2.5-GHz local clock signal. The divider must be capable of high frequency of operation and low input-sensitivity while consuming minimal power. Also the dividers should be synchronized between receivers to reduce the clock skew. The design and implementation of high-frequency CMOS frequency dividers are presented in Chapter 4. This section will present a design methodology based on injection locking for dividers implemented with source-coupled logic (SCL). These dividers oscillate in the absence of an input signal; hence, this oscillation can be injection-locked to provide frequency division from a low input-swing voltage signal. Measured results of SCL dividers operating up to 10 and 15.8 GHz, at 2.5 and 1.5 V, using 0.25- and 0.18-μm CMOS technologies are presented. Also, a dual-phase dynamic pseudo-NMOS divider [Yan99a] implemented in a partially-scaled 0.1-μm CMOS technology is presented, which operates up to 18.75 and 15.4 GHz on SOI and bulk substrates at 1.5 V, respectively. Finally, an initialization and start-up methodology to synchronize the dividers in each clock receiver is presented, which allows for decreasing the systematic skew.

In Chapter 5, the system requirements for the wireless clock distribution system are developed, translating the clock metrics of skew and jitter into standard RF metrics. To maximize the power transfer from the clock source to the local clock system, matching, gain, and antenna requirements are discussed. Clock skew and jitter are then used to set requirements for the power-level at the input of the frequency divider, the signal-to-noise ratio (SNR) at the input of the frequency divider, the noise figure for the LNA with source-follower buffers, and an IIP3 for the LNA and source-follower buffers. The overall system requirements are summarized and tabulated.

The major goal of this research is to demonstrate the operation of a wireless clock distribution system and evaluate its feasibility. Chapter 6 tackles the first of these two goals by demonstrating the operation and plausibility of a wireless clock distribution system. First, an overview of antenna fundamentals is presented along with measured on-chip antenna characteristics for test-chips implemented in 0.25- and 0.18-μm CMOS technologies. Antenna transmission gain, phase, and impedance results for linear dipole, zigzag dipole, loop antennas, and antennas in direct contact with the substrate are presented. Two single-receiver interconnects and one single-transmitter interconnect are then presented, demonstrating wireless interconnects for the first time. These interconnects operate at 7.4 GHz across 3.3 mm using the 0.25-μm technology and at 15 GHz across 5.6 and 6.8 mm using the 0.18-μm technology. Also, a double-receiver wireless interconnect with a programmable divider is demonstrated, and the clock skew and jitter are obtained.

Chapter 7 evaluates the feasibility of a wireless clock distribution system in terms of power consumption, process variation, synchronization, latency, area, and design verification. The worst-case clock skew and jitter are estimated and compared to the measured skew and jitter presented in Chapter 6. This chapter will show that comparable power consumption, skew, and jitter can be obtained with a wireless clock distribution system, as compared to conventional systems, with potential costs of added area and more difficult design verification. Finally, this chapter contains conclusions on the overall feasibility of a wireless clock distribution system and on this work in general, and suggests future work.

CHAPTER 2
CMOS LOW NOISE AMPLIFIERS

2.1 Overview

2.1.1 Scope of LNA Research

A key building block for the clock receiver, as well as for the front-end of super-heterodyne and direct conversion receivers, is the low noise amplifier (LNA). Due to its moderate to high gain as well as its low noise figure, the LNA approximately sets the overall signal-to-noise ratio of the receiver by reducing the impact of noise from subsequent stages. This is equivalent to saying that when the LNA is properly designed, the total receiver noise figure is roughly that of the LNA. For a cascaded system, the total noise factor (F) and noise figure (NF) are given by the following formulas [Gon97]:

$$F = \frac{(S/N)_{input}}{(S/N)_{output}} = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \ldots, \text{ and} \tag{2.1}$$

$$NF = 10 \cdot \log(F), \tag{2.2}$$

where (S/N) is a signal-to-noise ratio, and F_i and G_i are the noise factors and available power gains, respectively, of individual stages in the receiver. As can be seen, the noise contributions from latter stages are divided by the total gain preceding them--a process known as “input-referring.” Thus, to minimize the total noise figure, the first stage in the receiver should amplify the input signal while adding minimal noise.

For the wireless interconnect application, a CMOS technology is required to be consistent with the ITRS. However, RF CMOS circuitry has only recently been under

investigation by researchers, with most of the research occurring at frequencies below 6 GHz. The limited work in CMOS is due to the stringent performance requirements of conventional wireless standards (e.g., Global System for Mobile (GSM) or Global Positioning Systems (GPS)), which has necessitated the use of GaAs or silicon bipolar technologies. However, CMOS technologies can potentially reduce the overall cost of the transceiver by allowing increased levels of integration, with the single-chip radio being an ultimate goal. For CMOS technology to compete with silicon bipolar or GaAs technologies for wireless applications, it must at least deliver the minimum necessary performance at a reduced system-level cost. From a performance standpoint, to be competitive with bipolar or GaAs LNAs, CMOS LNAs must equal or surpass their low power consumptions of approximately 10 mW and their low noise figures of approximately 2 dB [Sha97]. From a cost standpoint, the LNA should be implemented in a standard digital CMOS technology without any specialty passive components, and the LNA should require a minimal number of external components.

While recent works have demonstrated the potential of CMOS LNAs for ~1-GHz applications, they generally have difficulty in attaining both low noise figure and low power consumption simultaneously [Sha97, Stu98, Hua98]. Alternately, if they do meet the low noise and low power, it is made possible by using either modified CMOS technologies or external matching networks [Gra00, Hay98]. Also, at this time, other than work that the author has participated in or originated, CMOS LNAs operating above ~5.8 GHz have not been reported. The following two chapters present the design and implementation of CMOS LNAs operating between 0.9 and 24 GHz. An explicitly defined design methodology is presented in this chapter which considers gain, noise figure, input

matching, and output matching. Implementation results for four different LNAs, operating at 0.9, 8, 14, and 23.8 GHz, respectively, are then presented in the next chapter.

2.1.2 Performance Metrics of LNAs

As mentioned above, to minimize the receiver's noise figure, the LNA is required to have moderate to high gain and low noise figure. Examining (2.1), it would seem that the LNA's gain can be increased arbitrarily, thereby minimizing the noise figure and improving the sensitivity of the receiver. However, this is not the case due to the effect of LNA gain on receiver linearity. Linearity is typically measured in terms of a third-order intercept point (IP3) which is usually input-referred (IIP3). The IP3 is the output power at which the third-order intermodulation products are equal to the desired linear component. The expression for the total IIP3 for a cascaded system can be expressed as follows:

$$\frac{1}{IIP3_T} = \frac{1}{IIP3_1} + \frac{G_1}{IIP3_2} + \frac{G_1 G_2}{IIP3_3} + \dots , \tag{2.3}$$

where $IIP3_i$ and G_i are the input-referred IP3 (in watts) and the power gain (in watts/watt) of each individual stage of the receiver. For gains greater than one, the linearity of latter stages will dominate the total receiver linearity. Therefore, to maximize the receiver's IIP3, the latter stages' linearity should be maximized while reducing or limiting the total preceding gain. Thus, the gain of the LNA (i.e., G_1) cannot be increased arbitrarily, since that would degrade the receiver's IIP3. Therefore, (2.1) and (2.3) imply an acceptable range of LNA gains which will meet both the system's noise figure and linearity requirements. Also from (2.3), it can be seen that the requirement for the LNA's IIP3 is not as stringent as that for subsequent stages (e.g., mixer). Typically, the LNA is designed to have a power gain of approximately 15 dB, a noise figure of less than 2 dB, and an IIP3 of -5 dBm, all the while consuming less than ~10 mW of power.

In superheterodyne and direct-conversion receivers, the LNA is preceded by the antenna, a duplexer filter or transmit/receive switch, and an optional pre-select filter. Since these components are not typically integrated, the input to the LNA is driven through a 50-Ω transmission line. Therefore, the LNA's input should be matched to 50 Ω. For the wireless clock receiver application, the input of the LNA should be conjugately matched to the antenna impedance, since transmission lines are not required. The output matching of the LNA depends on whether the LNA drives an off-chip component, such as an image-reject filter for superheterodyne architectures, or an on-chip component, such as a mixer for direct-conversion architectures or a frequency divider for the clock receiver application. When driving an off-chip component, the LNA's output should be matched to 50 Ω. The input and output matching criteria for a 50-Ω match are specified in terms S_{11} and S_{22}, where both should be less than -10 dB.

2.2 Possible LNA Topologies

Designing an LNA consists of meeting the gain, noise, matching, and linearity performance metrics while minimizing power consumption and cost (where all of the aforementioned tend to trade-off to a certain extent with one another). Towards this end, there are two main circuit topologies for CMOS that will be discussed--common-gate and common-source with inductive degeneration.

2.2.1 Common-Gate CMOS LNA

The first possible topology employs a common-gate amplifier with source inductance, shown in Figure 2-1(a). Appendix A contains derivations for the input impedance, gain, and noise figure for this common-gate topology. Here, the input is a parallel resonant

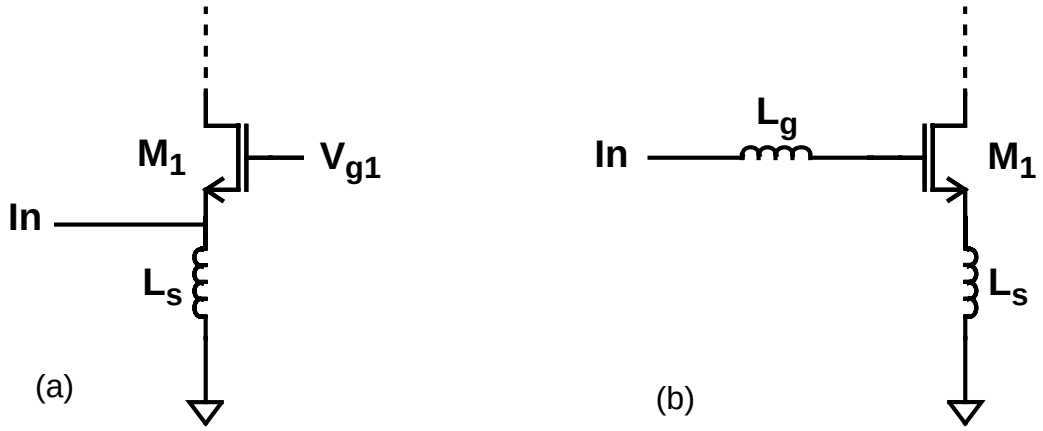


Figure 2-1 Potential CMOS LNA topologies: (a) common-gate or (b) common-source with inductive degeneration.

network composed essentially of the source inductance (L_s), the gate-to-source capacitance (C_{gs}), and one over the transconductance ($1/g_m$). The input impedance is designed to be ~50 Ω; however, to maximize the gain and minimize the noise figure, the input impedance can be set to ~35 Ω, while still achieving an S_{11} of -15 dB. Thus, g_m is set to approximately 1/35 Ω^{-1}, while L_s is chosen to parallel-resonate with C_{gs} at the operating frequency. In addition to easily providing the input match, the common-gate topology exhibits good linearity, due to the source degeneration of the transistor provided by R_S.

A drawback of this topology is its higher noise figure. As shown in Appendix A, the noise factor for this topology is approximately the following:

$$F = 1 + \frac{\gamma}{\alpha} \cdot \left(\frac{1}{g_m R_S} \right), \tag{2.4}$$

where α is the ratio between the device transconductance (g_m) and the short-circuit drain conductance (g_{d0}). In the long-channel limit, γ and α are 2/3 and 1, respectively, while γ can be significantly larger than 2/3 for short channel lengths, due to hot-electron effects [Jin85]. Thus, in the long-channel limit and with g_m=1/35 Ω^{-1}, the noise factor is 1.47, yielding a noise figure[1] of 1.66 dB. However the noise figure can be significantly larger in

the short-channel regime and when taking into account other sources of noise (e.g., substrate resistance, inductor parasitic resistance, and gate-induced noise [Zie86, Sha97, Tsi99]), with typical experimental values exceeding 3 dB.

The high noise figure for the common-gate topology is a major disadvantage. Fundamentally, the high noise figure is due to g_m being constrained by the input matching condition, which thereby constrains the noise figure. This is analogous to saying that the input matching conditions for optimal power match and noise match are not coincident. Therefore, a topology which decouples g_m from the input matching condition would add an additional degree of freedom to the design, and hopefully superimpose the power and noise matching conditions. A topology which provides this decoupling is shown in Figure 2-1(b), which consists of a common-source amplifier with inductive degeneration. To obtain the extra degree of freedom in the design, an inductor (L_g) is added in series with the gate. As will be shown in the next section, this topology allows the power and noise matching conditions to be met simultaneously, while exhibiting sufficient linearity and allowing for low power consumption.

2.2.2 Source-Degenerated CMOS LNA

Figure 2-2 shows a simplified schematic of a CMOS LNA with inductive source degeneration. This LNA is matched to 50 Ω at both the input and the output. A single-stage topology is used to minimize the power dissipation and to improve 1-dB compression point (P_{1dB}) and IP3 performance. The circuit gain is provided by a cascode

1. If $g_m = 1/50\ \Omega^{-1}$, then the noise figure would be approximately 2.2 dB for the long-channel limit.

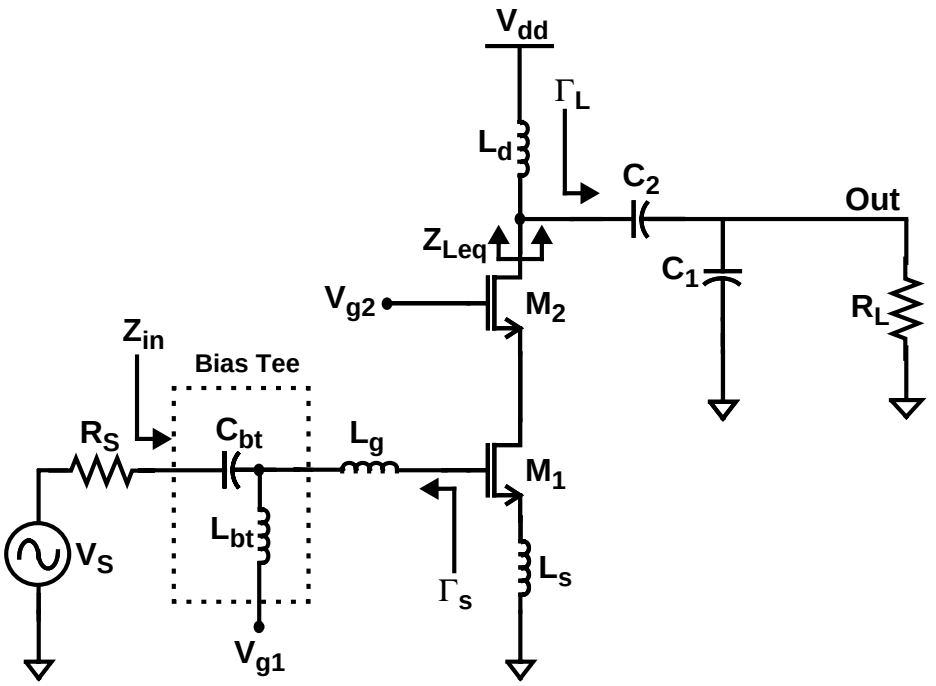


Figure 2-2 Schematic of the source-degenerated CMOS LNA

amplifier, which has a reduced Miller effect. Also, a cascode exhibits high reverse isolation, which simplifies the design procedure by decoupling the input and output matching conditions. While this topology is similar to other reported CMOS LNAs, fundamental differences include the omission of a 50-Ω output buffer, the use of shielding structures, and the use of a capacitive transformer at the output.

2.3 Input Matching for Source-Degenerated LNA

2.3.1 Input Impedance

It can readily be shown that the input impedance of the source-degenerated LNA, neglecting gate-to-drain capacitance (C_{gd1}), is as follows:

$$Z_{in} = j\omega(L_g + L_s) + \frac{1}{j\omega C_{gs1}} + \frac{g_{m1}}{C_{gs1}}L_s. \qquad (2.5)$$

A salient feature of this topology is that source degeneration provides a real term to the input impedance, which can then be used to match to 50 Ω. This real term is not a resistance *per se* (hence it will not generate thermal noise), but rather when a current is applied to the input node, the voltage that develops at that node has components both in phase (real term) and ±90 degrees out of phase (imaginary terms due to L_g, L_s, and C_{gs1}). The in-phase component results from the series feedback in the source of M_1.

As can be seen from (2.5), this network takes the form of a series resonant circuit, with resonant frequency

$$\omega_o = [(L_g + L_s)C_{gs1}]^{-\frac{1}{2}}. \tag{2.6}$$

Thus, at series resonance, the input impedance becomes

$$Z_{in} = \frac{g_{m1}}{C_{gs1}} L_s \approx \omega_T L_s, \tag{2.7}$$

which is a function of the bias condition, the channel length of M_1, and L_s. The quality factor of this network, including the source resistance, R_S, is

$$Q_{in} = \frac{1}{\omega_o C_{gs1} \cdot (R_S + \omega_T L_s)}. \tag{2.8}$$

Thus, to design the input matching network for a given C_{gs1} to achieve an S_{11} < -10 dB and series resonance, the following relations are used:

$$\frac{26}{\omega_T} < L_s < \frac{96}{\omega_T} \tag{2.9}$$

$$L_g = \frac{1}{\omega_o^2 C_{gs1}} - L_s. \tag{2.10}$$

2.3.2 Input Match to Withstand Component Variations

A methodology is then needed to choose C_{gs1} (i.e., the width of M_1) and yield L_s and L_g. One way is to choose C_{gs1} to meet the input matching condition over an entire

operating frequency band, while withstanding component variations in L_g, L_s, and C_{gs1}. Qualitatively, the input impedance is more sensitive to component variations for high-Q networks. Thus, there is a maximum value for the quality factor which ensures matching for a given frequency band and for a given set of component tolerances. An alternative input quality factor independent of L_s can be defined as follows:

$$Q_{gs} = \frac{1}{\omega_o C_{gs1} R_S}. \tag{2.11}$$

Assuming that inductors have a tolerance of T_L, C_{gs1} has a tolerance of T_C, and ω_T has a tolerance of T_T, equation (2.5) becomes the following:

$$\begin{aligned} Z_{in} &= \omega_T L_s(1 \pm T_L)(1 \pm T_T) + j\omega(L_g + L_s)(1 \pm T_L) + \frac{1}{j\omega C_{gs1}(1 \pm T_C)} \quad . \\ &= \omega_T L_s(1 \pm T_L)(1 \pm T_T) + jQ_{gs}R_s\left(\frac{\omega}{\omega_o}(1 \pm T_L) - \frac{\omega_o}{\omega}\frac{1}{(1 \pm T_C)}\right) \end{aligned} \tag{2.12}$$

Note that the variation in ω_T (which has a $|v_{sat}|/L$ dependence in the velocity-saturated regime [Tsi99], where v_{sat} is the saturation velocity) is partially correlated to the variation in C_{gs} (which has a WLC_{ox} dependence), through variations in the length of the device. The impedance in (2.12) has to satisfy the input matching condition at both the upper and lower ends of the frequency band (i.e., $\omega = \omega_o \pm \frac{B}{2}$, where B is the total bandwidth). The input impedances which satisfy S_{11} < -10 dB, can be visualized on a Smith chart as those impedances located within a circle centered at the origin with radius 0.32 ($10^{-10/20}$), as shown in Figure 2-3. If the input impedance is normalized and written as $z_{in}=(r)+j(i)$, the required value for i to result in a specific S_{11} for a given value of r is as follows:

$$i = \pm\sqrt{\frac{|S_{11}|^2(r+1)^2 - (r-1)^2}{1 - |S_{11}|^2}}. \tag{2.13}$$

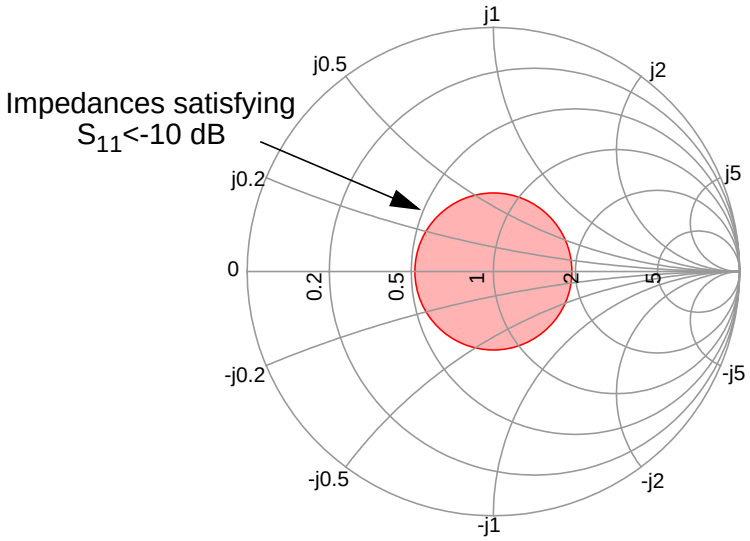


Figure 2-3 Smith chart showing impedances which satisfy S_{11}< -10 dB.

The worst case matching condition occurs either at the lower end of the frequency band when the component tolerances cause the resonant frequency to increase or at the upper end of the frequency band when the component tolerances cause the resonant frequency to decrease. Both conditions yield approximately the same value for Q_{gs}. Looking at the first condition (i.e., $L=L(1-T_L)$, $C_{gs1}=C_{gs1}(1-T_C)$, $\omega = \omega_o-\frac{B}{2}$, and $\omega_T=\omega_T(1-T_T)$), the required value of Q_{gs} can be solved by normalizing (2.12) and then applying (2.13), as follows:

$$Q_{gs} = \frac{\sigma(1-T_C)}{(1-\sigma^2(1-T_L)(1-T_C))}\sqrt{\frac{|S_{11}|^2(r+1)^2-(r-1)^2}{1-|S_{11}|^2}}, \qquad (2.14)$$

where

$$r = \frac{\omega_T L_s}{R_s}(1-T_L)(1-T_T), \qquad (2.15)$$

$$\sigma = \frac{\omega}{\omega_o}\bigg|_{\omega=\omega_o-\frac{B}{2}} = \frac{2Q_B-1}{2Q_B}, \qquad (2.16)$$

$$Q_B = \frac{\omega_o}{B}. \qquad (2.17)$$

Table 2-1 Required Value of Q_{gs} for Component Variations with S_{11} < -10 dB

Band	GSM 935-960 MHz	GSM 935-960 MHz	GSM 935-960 MHz	ISM 2.4-2.5 GHz	ISM 2.4-2.5 GHz	ISM 2.4-2.5 GHz
Q_B	37.9	37.9	37.9	24.5	24.5	24.5
$\|T_L\|$, $\|T_C\|$, $\|T_T\|$	5%	5%	10%	5%	5%	10%
$\omega_T L_s$	35	50	50	35	50	50
Q_{gs}	2.9	4.8	2.4	2.6	4.3	2.3

Table 2-1 shows the required value of Q_{gs} for the GSM and ISM (Industrial, Scientific, and Medical) bands, for varying component tolerances and values for $\omega_T L_s$. It can be seen that as Q_B (the quality factor implied by the operating frequency band) decreases, so too does Q_{gs}, as expected. Also, as the component tolerance becomes larger, the required value of Q_{gs} decreases, indicating that high-Q networks are more sensitive to component variations, as originally asserted. Finally, as $\omega_T L_s$ becomes closer to 50 Ω, Q_{gs} increases, indicating that the network can withstand larger component variations. Note that choosing a smaller value of Q_{gs} will result in additional margin for input matching variations. The results presented in Table 2-1 show that choosing Q_{gs} between 2.3 and 4.8 will result in S_{11} < -10 dB over the entire band, while withstanding between 5 to 10% of component variations. Once Q_{gs} is specified, C_{gs1} and hence W_1 can be determined, allowing the inductor values to be chosen as given by (2.9) and (2.10).

2.4 Output Matching for Source-Degenerated LNA

Driving a 50-Ω load while providing sufficient power gain requires either an output matching network or a 50-Ω buffer. Since a buffer typically would dissipate additional power while also degrading the circuit linearity, a single-stage design with an output

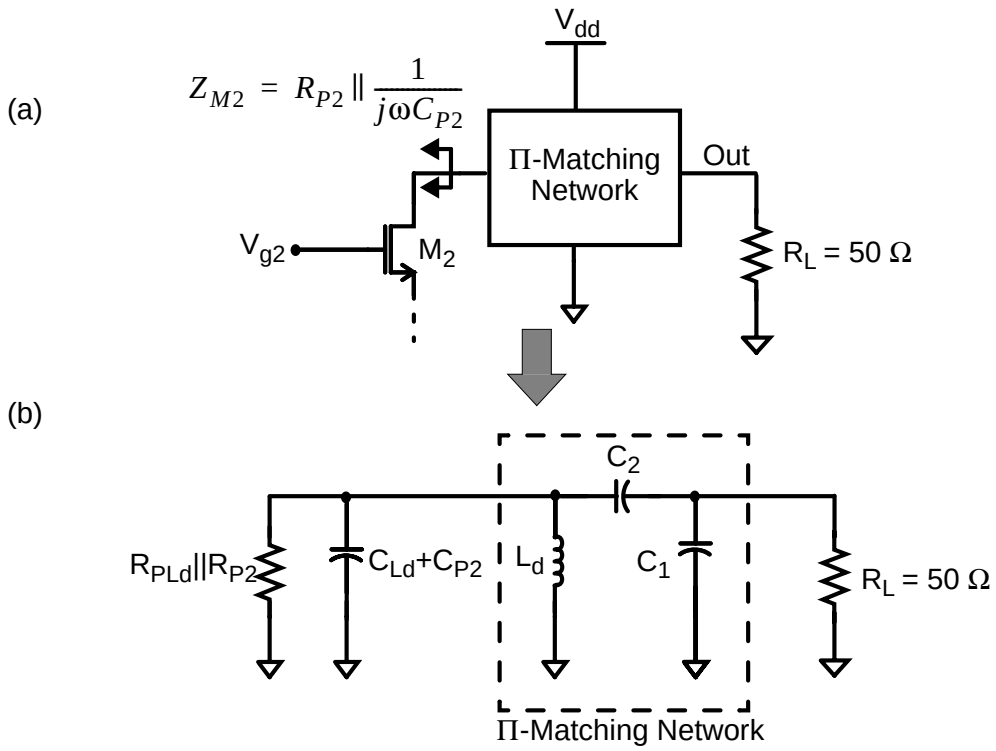


Figure 2-4 Output matching equivalent circuits for CMOS LNA

matching network is preferable. As shown in Figure 2-2 and Figure 2-4(a), the output impedance of M_2 is transformed to 50 Ω using a three-element matching network consisting of a capacitive transformer (C_1 and C_2) and a shunt inductor (L_d). This three-element network is also known as a Π matching network. Compared to a two-element matching network (or "L" network), a Π network allows multiple sets of component values for L_d, C_1, and C_2. Each set corresponds to a different loaded quality factor for the Π network. The two-element network, on the other hand, allows only one set of component values for L_d and C_2 (C_1 is no longer present), with the quality factor of the loaded network fixed by the impedance transformation ratio [Bow82]. Therefore, the Π network provides added flexibility to the designer, allowing multiple values for the drain inductor.

Figure 2-4(b) shows an equivalent circuit for the output matching network, including the parasitic series resistance (r_{Ld}) and shunt capacitance (C_{Ld}) associated with L_d. The output impedance of the cascode is represented as a resistance R_{P2} (on the order of kilo-ohms), in parallel with a capacitance C_{P2}, where C_{P2} consists of C_{gd2} and C_{db2}. For optimal power transfer, the matching network would transform R_{P2} to 50 Ω. However, this implies a quality factor of $Q \cong \sqrt{R_{P2}/50 - 1}$ for the matching network, which is on the order of 10 for $R_{P2} \cong 5$ kΩ. Since the matching network includes an on-chip spiral inductor, the quality factor of the network is limited by that of the inductor, Q_{Ld}. To include the finite Q of the spiral inductor, r_{Ld} can be transformed to an equivalent resistance shunting the inductor, as follows:

$$R_{PLd} = (Q_{Ld}^2 + 1) r_{Ld} \cong Q_{Ld}^2 r_{Ld}. \qquad (2.18)$$

Since R_{PLd} is typically much less than R_{P2}, the matching network transforms a complex source, consisting of R_{PLd} in parallel with the capacitance C_{P2}+C_{Ld}, into the 50-Ω load.

A dilemma now appears, in that the impedance to be transformed (R_{PLd}) is a function of the network providing the impedance transformation (L_d). Therefore, an iterative approach can be taken using gain and output matching as criteria, as follows: (1) an initial value is chosen for L_d, (2) R_{PLd} and C_{Ld} are then estimated along with Z_{M2} in Figure 2-4(a), (3) values for C_1 and C_2 are designed to achieve a 50-Ω match, and (4) S_{21} and S_{22} are checked against their specifications and L_d is updated if necessary. The initial value for L_d is chosen based on the desired gain, using formulas derived in the next section. The equations for C_1 and C_2 can be readily derived [Ho00], and are given in Appendix B. Thus, any standard two-element matching technique can be used to choose C_1 and C_2 for completing the match of Z_{M2} to 50 Ω (e.g., [Bow82]).

2.5 Gain of Source-Degenerated LNA

For an amplifier driven by a source V_S, with source impedance R_S, and loaded at the output by R_L via transmission lines with characteristic impedances of R_S and R_L, respectively, the forward transducer power gain is given by [Gon97]

$$G_T = \frac{P_{Load}}{P_{AVS}} = |S_{21}|^2 = 4\left|\frac{V_{Out}}{V_S}\right|^2 \cdot \frac{R_S}{R_L} = 4|A_v|^2 \cdot \frac{R_S}{R_L}, \tag{2.19}$$

where P_{Load} is the power delivered to the load, and P_{AVS} is the power available from the source. For R_S=R_L=50 Ω, the transducer power gain is then

$$G_T = |S_{21}|^2 = |2 \cdot A_v|^2. \tag{2.20}$$

2.5.1 Gain Driving Resistive Load

It can be shown that the voltage gain from the source to the load, A_v, assuming that the input is at series resonance and again neglecting C_{gd1}, is as follows:

$$\begin{aligned} |A_v|_{\omega = \omega_o} &= \left|\left(\frac{V_{gs1}}{V_S}\right)\left(\frac{V_{d1}}{V_{gs1}}\right)\left(\frac{V_{d2}}{V_{d1}}\right)\left(\frac{V_{Out}}{V_{d2}}\right)\right| \\ &= (Q_{in})\left(\frac{g_{m1}}{|g_{m2} + j\omega_o C_{d1}|}\right)(g_{m2}|Z_{Leq}(\omega_o)|)\left(\left|\frac{j\omega_o C_2 R_L}{1 + j\omega_o (C_1 + C_2) R_L}\right|\right) \end{aligned} \tag{2.21}$$

where C_{d1} is the total capacitance at the node connecting the drain of M_1 to the source of M_2, and Q_{in} is the quality factor of the input series resonant circuit, as given by equation (2.8). Here, Z_{Leq} is the total equivalent impedance at the drain node of M_2, as shown in Figure 2-2. Since the output matching network essentially matches the equivalent parallel resistance of inductor L_d to the load resistance, R_L, then Z_{Leq} is approximately equal to the following:

$$Z_{Leq}(\omega_o) \cong \frac{1}{2} Q_{Ld}^2 r_{Ld} = \frac{1}{2} Q_{Ld} \omega_o L_d. \tag{2.22}$$

The voltage gain can then be written as

$$\left|A_v\right|_{\omega = \omega_o} = \frac{1}{2} \cdot Q_{in} \cdot g_{m1} \cdot (Q_{Ld} \cdot \omega_o \cdot L_d) \cdot \left|\frac{\delta(\omega_o)}{n(\omega_o)}\right|, \tag{2.23}$$

where

$$\delta(\omega) = \frac{g_{m2}}{g_{m2} + j\omega C_{d1}} \tag{2.24}$$

$$n(\omega) = \frac{1 + j\omega(C_1 + C_2)R_L}{j\omega C_2 R_L}. \tag{2.25}$$

Here, $\delta(\omega)$ is a low-pass filter response, where the low-pass filter is composed of C_{d1} and $1/g_{m2}$; $n(\omega)$ is a complex capacitive transformer ratio. At sufficiently high frequencies, $n(\omega)$ reduces to $1+\frac{C_1}{C_2}$; however, this approximation must be justified and is rarely appropriate for typical values of C_2. By inspection, the ratio $|\delta/n|$ is always less than 1. Further simplification can be applied to (2.23) to obtain a more useful equation. Substituting (2.8) and noting that $\omega_T \cong g_{m1}/C_{gs1}$, it can be shown that

$$\left|S_{21}\right| = 2 \cdot \left|A_v\right|_{\omega = \omega_o} = \left(\frac{\omega_T \cdot Q_{Ld} \cdot L_d}{R_S + \omega_T L_s}\right) \cdot \left|\frac{\delta(\omega_o)}{n(\omega_o)}\right|. \tag{2.26}$$

2.5.2 Methods to Maximize Gain

To maximize the gain (S_{21}), four steps can be taken. First, examining the effect of the drain inductor on S_{21} requires examining the term $Q_{Ld}L_d/n(\omega_o)$, where $n(\omega_o)$ depends on Q_{Ld} and L_d via C_1 and C_2. However, since $n(\omega_o)$ is approximately a capacitance *ratio*, its dependence on Q_{Ld} and L_d is weak. Therefore, S_{21} increases with increasing Q_{Ld} and increasing L_d. This can be seen in Figure 2-5, where S_{21} is plotted (a) versus L_d for constant Q_{Ld} and (b) versus Q_{Ld} for constant L_d. For each data point, the output is matched to 50 Ω. Therefore, the LNA should be designed such that L_d and its quality

factor is maximized[2]. Second, to maximize the gain, ω_T should be maximized. This can be achieved in two ways, as follows: (1) bias the transistor for maximum ω_T, which can increase the power consumption, or (2) use a more advanced (i.e., costly) technology (shorter channel length) for a given power consumption. Thus, cost and power consumption should be balanced to achieve the correct trade-off for ω_T. Third, looking in the denominator of (2.26), it can be seen that the gain and the input matching criteria trade-off via the term $\omega_T L_S$. Since series feedback is used in the source of M_1, the gain is reduced while the input series resistance (R_S) is increased by a factor of one plus the loop gain ($1+\omega_T L_s/R_S$). Returning to (2.9), the input matching condition can still be met by choosing $\omega_T L_s \cong 35\ \Omega$, as opposed to 50 Ω. Thus, by allowing a small amount of mismatch at the input (i.e., S_{11} = -15 dB), the gain is increased by approximately 18%, or 1.4 dB. Finally, the term $|\delta/n|$ should be maximized, where δ can be maximized by reducing C_{d1} through judicious layout, and *n* can be minimized by decreasing or even eliminating C_1.

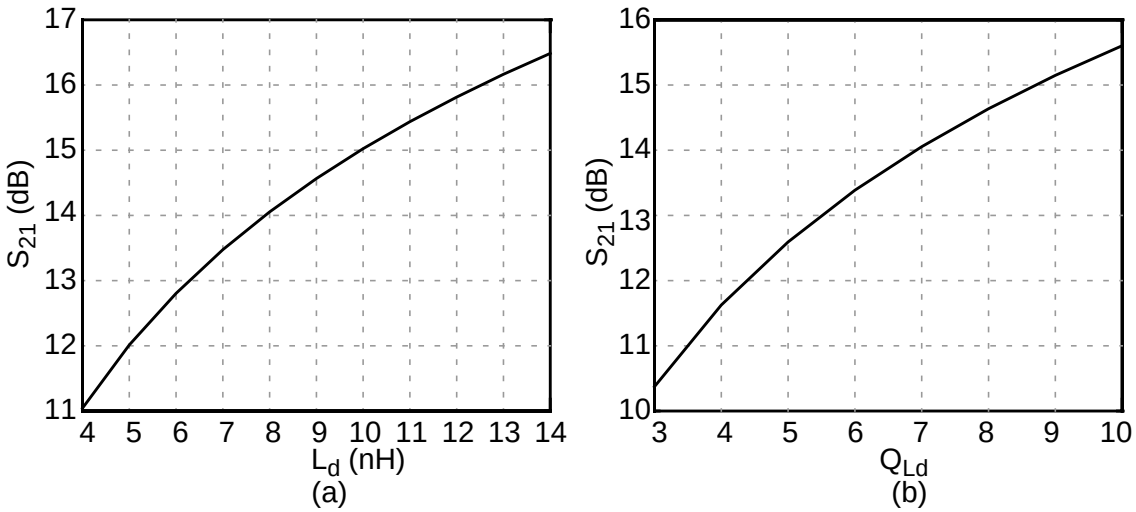


Figure 2-5 S_{21} at resonance versus (a) L_d for constant Q_{Ld} and (b) Q_{Ld} for constant L_d. The output is always matched to 50 Ω.

2. Note that if Q_{Ld} becomes too large, the LNA can become intolerant to process variations.

Looking at these four options, Q_{Ld} and ω_T have the most significant impact on gain. Intuitively, high-quality factor inductors result in LNAs which consume lower power. This is the case for [Hay98], where external matching networks are used to obtain high gain and low noise at a very small power. However, for a fully integrated LNA, external matching networks are taboo, since the extra components increase the cost and since their high Q's are not very repeatable. Thus, to obtain the desired gain using on-chip inductors with limited quality factors, the power consumption has to be increased. The quality factor of L_d is limited by the number of metal layers present, the oxide thickness between the top-level metal and the substrate, the substrate resistance, and the type of material used for the metal interconnect (aluminum or copper).

2.5.3 Gain Driving Capacitive Load

When the LNA does not drive 50 Ω, and instead drives a capacitive load (i.e., mixer or frequency divider), the gain is significantly increased. Thus, when the capacitive transformer (C_1 and C_2) is removed, Z_{Leq} consists only of the drain inductor with its parasitics in parallel with an equivalent load capacitance composed of C_{Ld}, C_{M2}, and the capacitance of the subsequent stage. Thus, $Z_{Leq}(\omega_o)$ becomes twice that given by equation (2.22). Also, with the output matching network removed, $n(\omega)$ is no longer required. The *voltage* gain then becomes the following:

$$\left|A_v\right|_{\omega = \omega_o} = 2 \cdot \left(\frac{\omega_T \cdot Q_{Ld} \cdot L_d}{R_S + \omega_T L_S}\right) \cdot \left|\delta(\omega_o)\right| . \qquad (2.27)$$

With the elimination of $n(\omega)$ and the additional factor of two, the gain can be significantly larger. This means that the desired gain of ~15 dB can be achieved at a reduced power consumption (i.e., ω_T). Also, since C_1 and C_2 are removed, the total capacitance resonating with L_d is small. Thus, L_d can be increased, further increasing the gain.

2.6 Noise Parameters

The noise factor of any two-port network can be classified in terms of four noise parameters as follows:

$$F = F_{min} + \frac{G_n}{R_S}[|Z_S - Z_{opt}|^2], \tag{2.28}$$

where F_{min} is the minimum obtainable noise factor, G_n is the noise conductance, $Z_{opt} = R_{opt} + jX_{opt}$ is the optimum source impedance resulting in $F = F_{min}$, and $Z_S = R_s + jX_S$ is the actual source impedance. Note that these noise parameters are more convenient than the four traditional noise parameters (F_{min}, R_n, G_{opt}, B_{opt}) [Gon97] for the source-degenerated LNA, due to the source being in an impedance form rather than an admittance form. A review of this set of noise parameters in impedance form is contained in Appendix C.

2.6.1 Noise Sources

The primary noise source within the CMOS LNA is thermal noise generated by the distributed channel of the MOS transistor. A secondary noise source is thermal noise generated by the series resistance of spiral inductors. Channel noise can be lumped into two current-noise sources--one at the drain and one at the gate. The drain noise-current has the following power spectral density:

$$\frac{\overline{i_d^2}}{\Delta f} = 4kT\gamma g_{do}, \tag{2.29}$$

where γ is a bias-dependent parameter (0.67 for long-channel devices), k is Boltzmann's constant (1.38×10^{-23} J/K), T is absolute temperature, and g_{do} is the short-circuit drain conductance. The gate noise-current, a second-order effect known as gate-induced noise (GIN) [Zie86, Sha97, Tsi99], has the following power spectral density:

$$\frac{\overline{i_g^2}}{\Delta f} = 4kT\delta\left(\frac{\omega^2 C_{gs}{}^2}{5g_{do}}\right), \tag{2.30}$$

where δ is another bias-dependent parameter (1.33 for long-channel devices). Since the origin of both the drain and gate noise currents is the channel, these noise sources are correlated, having a correlation coefficient (c) of j0.395 for long-channel devices. Due to the gate-to-channel capacitance providing a 90^o phase shift, c is complex.

Aside from GIN, there are three other second-order noise sources within the LNA, as follows: channel noise of M_2, thermal noise associated with gate resistance, and thermal noise generated in the substrate [Kis99]. To understand the relative importance of these second-order effects, the noise parameters for a single transistor will be derived in the following section.

2.6.2 Noise Parameters of Single Transistor

Figure 2-6 shows the high-frequency, quasi-static model for the intrinsic MOSFET [Tsi99], including noise sources. Deriving the noise parameters for this single transistor including drain and gate-induced noise, the body transconductance (g_{mb}), substrate

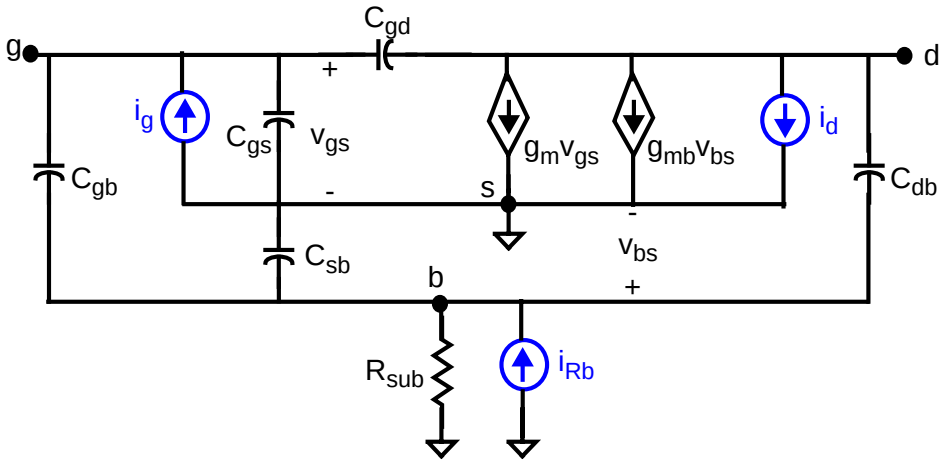


Figure 2-6 High-frequency, quasi-static model of intrinsic MOSFET.

resistance (R_{sub}), and all of the capacitances (C_{gs}, C_{gd}, C_{gb}, C_{db} and C_{sb}) is an arduous (albeit doable) task, yielding cumbersome equations. These equations can be found in Appendix D, both for the general case considering all second-order effects, as well as case-studies examining individual second-order effects. Rather than show these equations here, the resultant parameters are evaluated numerically using Matlab. Figures 2-7(a)-(d) show the effects of Q_{gs}, R_{sub}, each of the capacitances--gate-to-drain (C_{gd}), gate-to-body (C_{gb}), drain-to-body (C_{db}), and source-to-body (C_{sb})--and g_{mb} on derived noise parameters for a single MOS transistor with GIN turned on and off. Each noise parameter is plotted versus the following normalized parameters: Q_{gs} ranging from 0 to 10 with GIN both on and off (a first-order effect including width dependence of drain noise), R_{sub} ranging from 0 to 1000, and g_{mb}/g_m, $C_{gb}/C_{gs,}$ C_{gd}/C_{gs}, and $C_{db,sb}/C_{gs}$ each ranging from 0 to 1. The following are assumed: $\gamma = 1.2$, $\left(\frac{\omega_o}{\omega_T}\right) = \frac{1}{4}$, and $\delta = 2\gamma$. For each individual effect examined, the other parameters are held constant according to the assumptions listed in Figure 2-7.

The results for F_{min}, plotted in Figure 2-7(a) show a strong dependence on each of the effects considered. First, to reduce F_{min}, R_{sub} should be either very small (short) or very large (open). Substrate resistance can be minimized by surrounding the transistor with large-area substrate contacts very close to the channel. Second, to reduce F_{min}, the mechanisms which couple substrate noise into the transistor (i.e., g_{mb}, C_{gb}, and C_{db}) should in general be minimized, where C_{gb} and C_{db} are layout-dependent. Third, F_{min} decreases with increasing C_{gd}. This is due to feedback through C_{gd} decreasing the uncorrelated noise resistance, R_u, caused by GIN. Finally, since Q_{gs} is inversely proportional to device width, the channel thermal noise and the coupled substrate noise are reduced as Q_{gs}

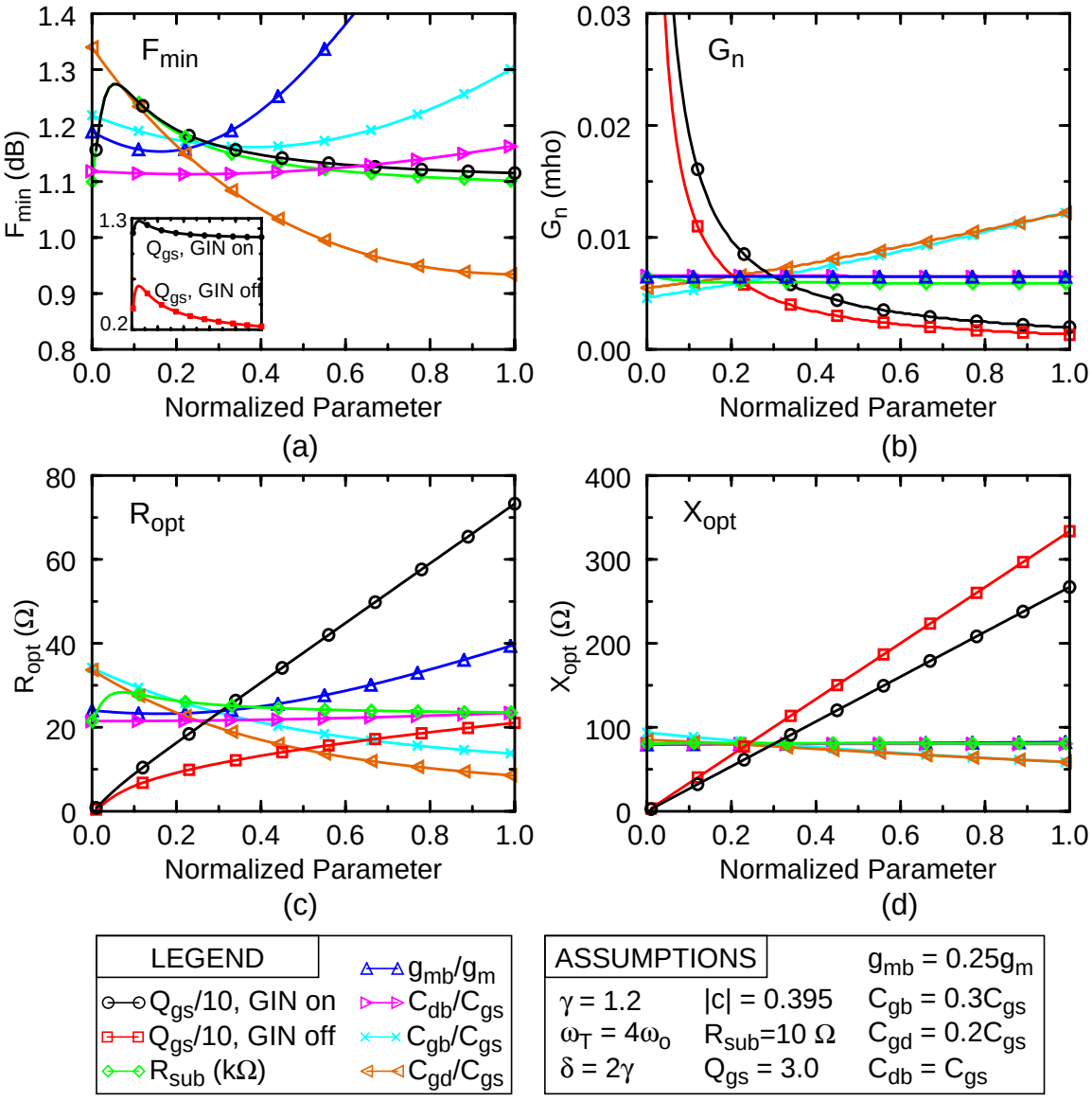


Figure 2-7 Noise parameters (a) F_{min}, (b) G_n, (c) R_{opt}, and (d) X_{opt}, for the following normalized parameters: Q_{gs} with GIN on and off, R_{sub}, g_{mb}, C_{db}, C_{gb}, and C_{gd}. For each parameter studied, all other parameters are held constant using the values listed in the assumption table, and GIN is on (except, obviously, for Q_{gs}, GIN off case).

increases. Therefore, F_{min} decreases accordingly. For very low values of Q_{gs}, F_{min} decreases due to the transistor and its parasitic capacitances being so large. Specifically, C_{sb} begins to shunt the substrate noise to ground, decreasing its contribution to F_{min}. The value of Q_{gs} for which F_{min} is maximum depends on the value of R_{sub}.

2.6.3 Optimum Q_{gs} for Minimum Noise

While F_{min} is strongly dependent on multiple effects (GIN, R_{sub}, g_{mb}, C_{gd}, and C_{gb}), G_n and X_{opt} are only strongly dependent on Q_{gs} with GIN on or off, and R_{opt} is only strongly dependent on Q_{gs} with GIN on. Therefore, only GIN and Q_{gs} need to be considered for G_n and Z_{opt}. With this simplification, a design procedure for minimum noise can be developed. First, F_{min} is minimized with respect to R_{sub} and each of the capacitances. Second, the actual noise factor (F) is minimized with respect to Q_{gs}, including the effects of GIN, through choosing the noise matching condition to approximately coincide with the power matching condition. Figure 2-8 shows F_{min} and F versus Q_{gs} with GIN on. Here, S_{11} is constrained to be -10 or -15 dB, with $\omega_T L_S$ set to 50 Ω. Constraining S_{11} prevents Z_s from being equal to $Z_{opt,}$ resulting in a higher noise figure. As can be seen from Figure 2-8, optimizing F with respect to Q_{gs} is much more valuable than optimizing F_{min}. Also, since F_{min} is relatively flat compared to F, only the quantity F-F_{min} has to be

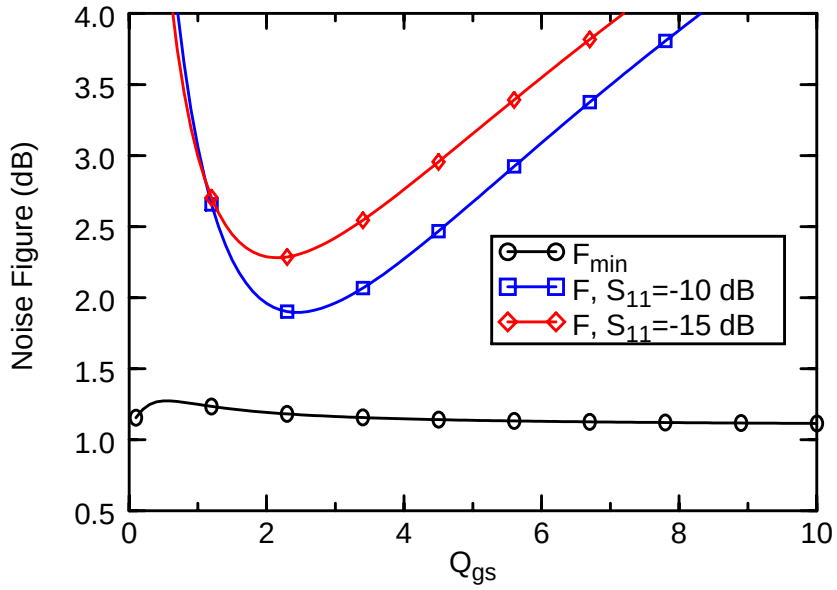


Figure 2-8 Minimum noise figure and actual noise figure when the input matching is constrained by S_{11}. The difference between F and F_{min} indicates that constraining S_{11} causes a noise mismatch.

optimized. From the results shown in Figure 2-7, it can be seen that F-F_{min} (a function of G_n, Z_{opt}, and Z_S) can be optimized considering GIN and Q_{gs} only.

The noise parameters of a cascode (M_1 and M_2) with and without source degeneration are shown in Table 2-2, including GIN for M_1. Here, $C_{gd1,2}$, gate and substrate

Table 2-2 Noise Parameters in Impedance Format

Cascode (M_1 and M_2)	Cascode with L_s
$G_n = \gamma_1 g_{do1}\left(\frac{\omega_o}{\omega_T}\right)^2 b_2 = \left(\frac{\gamma_1}{\alpha_1}b_2\right)\left(\frac{\omega_o}{\omega_T}\right)\cdot\frac{1}{Q_{gs}R_S}$ (2.31)	$G_n' = G_n$ (2.32)
$R_{opt} = \frac{\Delta\sqrt{\zeta-\lvert c\rvert^2}}{\omega_o C_{gs1} b_2} = \left(\frac{\Delta\sqrt{\zeta-\lvert c\rvert^2}}{b_2}\right)\cdot Q_{gs}R_S$ (2.33)	$R_{opt}' = R_{opt}$ (2.34)
$X_{opt} = \left(\frac{b_1}{b_2}\right)\frac{1}{\omega_o C_{gs1}} = \left(\frac{b_1}{b_2}\right)\cdot Q_{gs}R_S$ (2.35)	$X_{opt}' = X_{opt} - \omega_o L_s$ (2.36)
$F_{min} = 1 + 2\left(\frac{\omega_o}{\omega_T}\right)\frac{\gamma_1\Delta}{\alpha_1}\sqrt{\zeta-\lvert c\rvert^2}$ (2.37)	$F_{min}' = F_{min}$ (2.38)

resistance, $C_{gb1,2}$, and gate-induced noise of M_2 have all been neglected. The noise parameters for a single transistor under the same assumptions are derived in Appendix D, section D.3.2. The following variables have been introduced:

$$\zeta(W_2) = 1 + \frac{\gamma_2 g_{do2}}{\gamma_1 g_{do1}}\left(\frac{\omega C_{d1}}{g_{m2}}\right)^2, \tag{2.39}$$

$$\Delta = \sqrt{\frac{\delta_1 \alpha_1^2}{5\gamma}}, \tag{2.40}$$

$$b_1 = \zeta + \Delta|c|, \tag{2.41}$$

$$b_2 = \zeta + 2\Delta|c| + \Delta^2, \tag{2.42}$$

$$\alpha = \frac{g_m}{g_{do}}. \tag{2.43}$$

From (2.31),(2.33), and (2.35), it can be seen that G_n is inversely proportional to Q_{gs}, while R_{opt} and X_{opt} are directly proportional to Q_{gs}. This agrees very well with the noise parameters plotted in Figure 2-7.

Source degeneration modifies the noise parameters [Har73]. For the specific case corresponding to neglecting C_{gd} and transistor output impedance (the model used to calculate the original noise parameters), all but X_{opt} remain unchanged (a benefit of using impedance noise parameters). These modified noise parameters are also shown in Table 2-2. Through setting $\zeta = 1$ and $\delta_1 = 0$, the noise parameters for a single transistor, excluding GIN and R_{sub}, can be obtained. Examining (2.28),(2.31), and (2.37), it can be seen that as with the gain analysis, ω_T should be maximized to reduce noise figure.

These noise parameters for the source-degenerated cascode are substituted into (2.28), along with $Z_S = R_S + j\omega_o L_g$, yielding the following:

$$F - F_{min} = \frac{\gamma_1}{\alpha_1}\left(\frac{\omega_o}{\omega_T}\right)\frac{b_2}{Q_{gs}}\left\{\left[1 - Q_{gs}\frac{\Delta\sqrt{\zeta - |c|^2}}{b_2}\right]^2 + \left[Q_L - Q_{gs}\left(\frac{b_1}{b_2}\right)\right]^2\right\}, \tag{2.44}$$

where

$$Q_L = \frac{\omega_o(L_g + L_s)}{R_S}. \tag{2.45}$$

By inspection of (2.44), setting $Q_L = Q_{gs}$ (corresponding to series resonance at the input) does not result in minimum noise; thus, there is a trade-off between the noise matching and the power matching conditions. For a given value of S_{11} and assuming $\omega_T L_s = R_S$, the following required value of Q_L for minimum noise can be obtained through the aid of (2.13):

$$Q_L = Q_{gs} - \sqrt{\frac{4|S_{11}|^2}{1-|S_{11}|^2}}. \quad (2.46)$$

Thus, the input should be designed such that the series resonance occurs at a frequency higher than the operating frequency. Note that for S_{11} = 0, Q_L = Q_{gs}, as expected. Substituting (2.46) into (2.44), taking the partial derivative with respect to Q_{gs}, and setting the result to zero yields the optimum Q_{gs} for minimum F-F_{min} as follows:

$$Q_{gs}^{opt} = \sqrt{\frac{b_2}{\Delta^2}\left(1+\frac{4|S_{11}|^2}{1-|S_{11}|^2}\right)}. \quad (2.47)$$

For the assumptions listed in Figure 2-7 with S_{11} = -10 dB, and setting ζ=1, then Q_{gs}^{opt} equals 2.62 and Q_L is 1.95. For S_{11} = -15 dB, Q_{gs}^{opt} is 2.32 and Q_L is 1.96, while for S_{11} = -∞ dB, corresponding to a perfect input match, Q_{gs}^{opt} = Q_L = 2.18. At these optimal Q_{gs} values, F-F_{min} is 0.02, 0.07, and 0.17 for S_{11} = -10, -15, and -∞ dB, respectively[3], when considering GIN only (i.e., (2.44)). When considering all of the second-order effects (i.e., as in Figure 2-7), F-F_{min} is 0.24, 0.38, and 0.65, respectively[4]. Therefore, matching the input for perfect series resonance results in a higher NF, as is the case for [Sha97].

2.6.4 Optimum Width of M_2

The optimum sizing of M_2 can be obtained by minimizing $\zeta(W_2)$. Since g_{m2} and g_{do2} are directly proportional to W_2, while C_{d1} has components directly proportional to W_1 and to W_2, then $\zeta(W_2)$ has components proportional to and inversely proportional to

3. The impact in decibels depends on the particular value of F_{min}. For F_{min} = 1 dB, the corresponding noise figures are 1.1, 1.2, and 1.6 dB, respectively.

4. For F_{min} = 1 dB, the corresponding noise figures are 1.8, 2.2, and 3.8 dB, respectively.

W_2. Thus, an optimum value of W_2 exists which minimizes ζ. The capacitance at the drain of M_1 (C_{d1}) can be written as follows, neglecting interconnect capacitance:

$$C_{d1} \cong C_{d11} W_1 + C_{d12} W_2 , \tag{2.48}$$

where $C_{d11}W_1$ consists of C_{db1} plus a fraction of C_{gd1}, and $C_{d12}W_2$ consists of C_{sb2} and C_{gs2}. Differentiating (2.39) with respect to W_2 assuming constant drain current and constant V_{ds1} yields the following:

$$W_2 = \frac{C_{d11}}{C_{d12}} W_1 . \tag{2.49}$$

Thus, the capacitance at the drain-node of M_1 should be equally divided between M_1 and M_2. Figure 2-9 shows a plot of simulated noise factor versus W_2 for a 0.25-μm technology. For this simulation the default noise model for BSIM3v3 is being used. The optimum width of M_2 is 60 μm, when W_1 is set to 90 μm. Calculations show that for this same technology, the ratio C_{d11}/C_{d12} is equal to 0.6, yielding a calculated optimal W_2 of 53 μm.

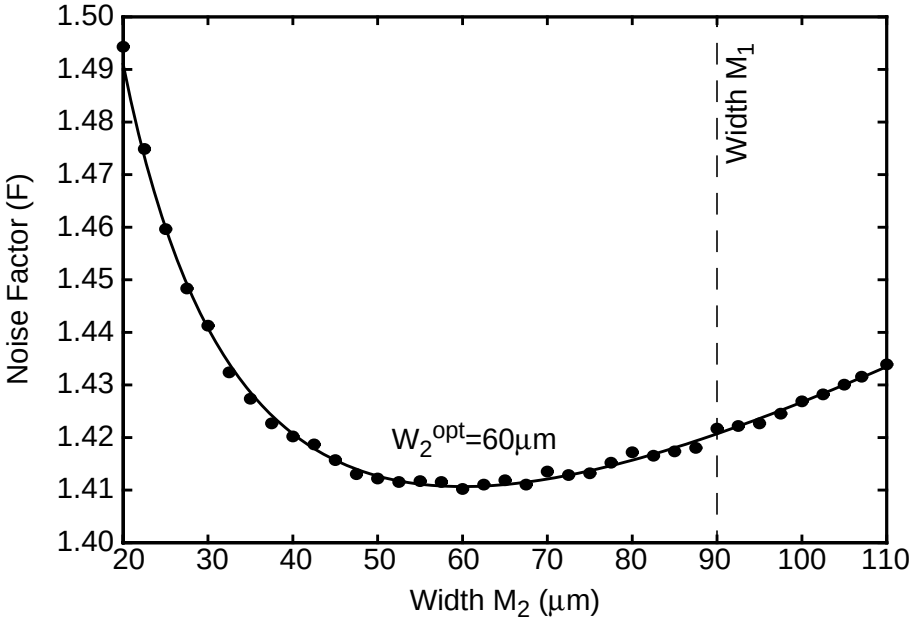


Figure 2-9 Noise factor versus width of cascoded transistor (M_2). The optimum width occurs when the capacitance at the intermediate node between M_1 and M_2 is equally balanced between M_1 and M_2.

Thus, the simulated and calculated optimal values for W_2 agree reasonably well. Also, as can be seen from Figure 2-9, choosing W_2/W_1 ranging from 0.55 to 0.75 will result in minimal noise contribution from M_2. Therefore, the noise parameters yield the optimum values for W_1 and W_2, through equations (2.47) and (2.49), respectively, as well as the optimum gate inductance for a given input reflection coefficient through equation (2.46).

2.7 Design Methodologies for Source-Degenerated LNA

2.7.1 Derivation-Based Methodology

Now, a complete design methodology based on the previous derivations has been developed for the source-degenerated CMOS LNA, assuming a given technology. First, choose Q_{gs} to be nominally 2.6. This value should be the minimum of those obtained from (2.14) and (2.47), yielding minimum noise and robustness against component variations. Once Q_{gs} is defined, W_1 can be determined based on C_{ox}. Second, using the gain and noise equations along with the desired power consumption, estimate the required ω_T, yielding an approximate operating point for M_1. Third, determine W_2 using (2.49). Fourth, set L_s nominally to $50/\omega_T$, where lower values can be used to slightly boost the gain while sacrificing input matching robustness. Fifth, determine L_g using (2.45) and (2.46) based on the desired value for S_{11}. Sixth, using gain equation (2.26), estimate the value of L_d needed to achieve a desired value for S_{21} (note, $|\delta/n|$ can be estimated to be ~0.2). Seventh, extract parasitics of L_d and cascode, and match the output to 50 Ω using any standard ideal matching technique, determining values for C_1 and C_2.

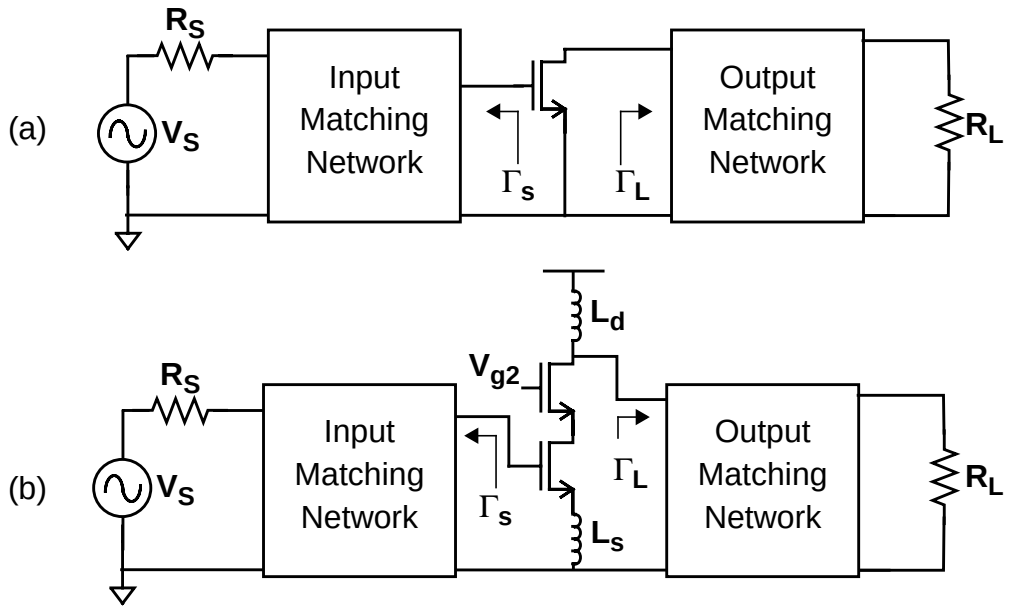


Figure 2-10 Illustration of constant available gain methods, where for the gain stage either, (a) a single transistor is used or (b) a source-degenerated cascode with inductive load is used.

2.7.2 Alternative Constant Available Gain Methodology

The above design methodology is sensitive to the derived noise parameters. As SPICE intrinsic noise models continue to improve, it is easier and "more" accurate to use CAD tools to obtain the noise parameters of an intrinsic model with additional extrinsic parasitics also modeled. A methodology for choosing L_g, C_1, and C_2 well-suited to CAD, is the constant available gain method. Traditionally, the constant available gain method is used to generate ideal matching networks, when given the S-parameters and noise parameters of a single transistor [Gon97], as illustrated in Figure 2-10(a). However, since lossy inductors are used at both the drain and the source, a composite circuit including L_s, L_d, and the cascode is used in place of the active device, as illustrated in Figure 2-10(b). Values for W_1, W_2, L_s and L_d are chosen using the previous methodology. The S-parameters and noise parameters of the composite circuit including the inductors are extracted using

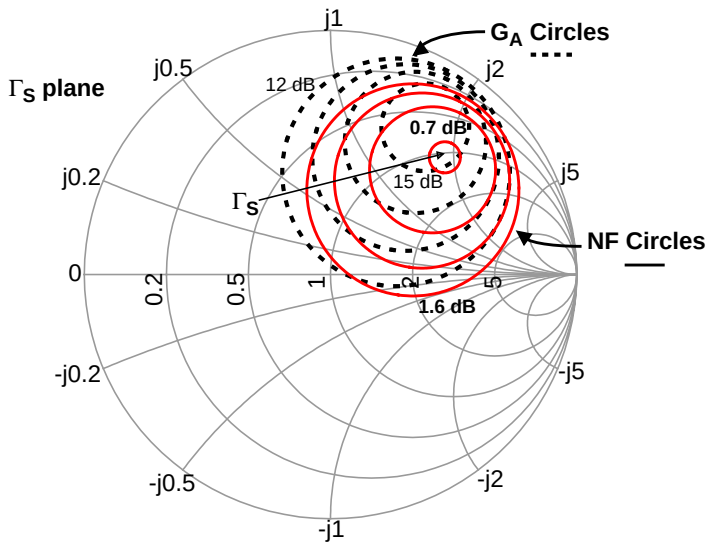


Figure 2-11 Constant available gain and NF circles for cascode with L_s and L_d.

SPICE. Using these parameters, constant available gain (G_A) circles and constant noise circles are plotted on the Smith chart, along with input and output stability circles. Using these circles, the reflection coefficient of the source and the load, Γ_S and Γ_L, can be determined. Once Γ_S and Γ_L are determined, the input and output matching networks can readily be designed.

Figure 2-11 shows a plot of simulated constant gain and noise circles on the Smith chart. Assuming Q_{gs} is chosen using (2.47), R_{opt} should be close to the 50-Ω circle. The value of L_g closest to Γ_{opt}, while still meeting the desired S_{11} specification, can then be read off the Smith chart. The output is then conjugately matched (i.e., $\Gamma_L = \Gamma_{out}^*$), using the following formula:

$$\Gamma_{out} = \Gamma_L^* = S_{22} + \frac{S_{21}S_{12}\Gamma_S}{1 - S_{11}\Gamma_S}. \tag{2.50}$$

This determines the output matching network, the simplest of which is a capacitive transformer, C_1 and C_2. To obtain C_1, a constant conductance circle is traversed from the center of the Smith chart, while to obtain C_2, a constant resistance circle is traversed from the endpoint of the previous path to $\Gamma_L=\Gamma_{out}^*$, as shown in Figure 2-12.

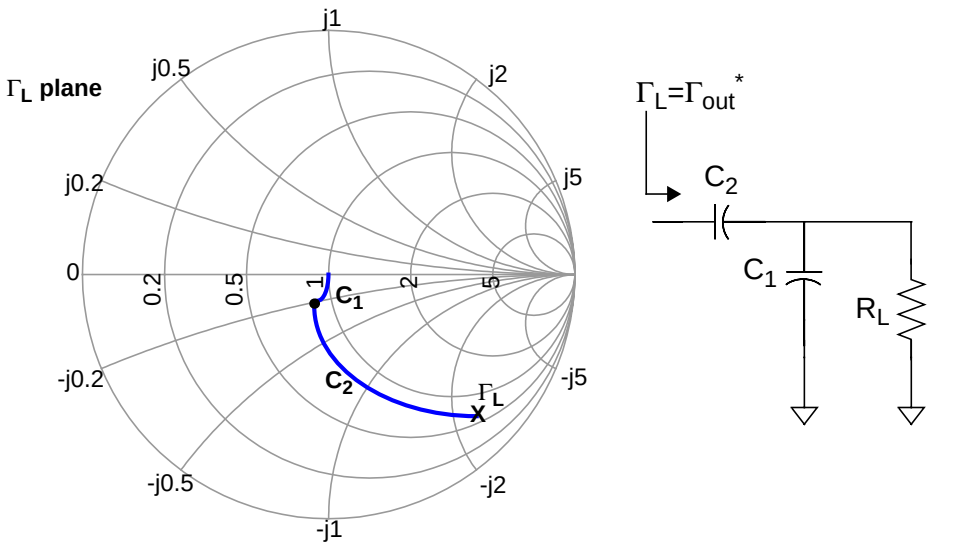


Figure 2-12 Output matching network design to match 50 Ω to Γ_{out}^{*}.

2.8 Summary

Common-gate and source-degenerated LNAs have been presented. An explicit design methodology has been developed for a source-degenerated CMOS LNA, considering gain, NF, input matching, and output matching. In particular, the optimal sizing of the transistors has been presented for robustness against input matching variations and for minimal noise figure. The noise parameters (in impedance form) for a MOSFET have been derived to understand the effect of various second-order effects on noise performance. Gate-induced noise and substrate resistance both affect the noise parameters significantly. Using these results, a design methodology for minimum noise while constraining the input matching condition has been presented, which yields an optimal value for the size of the primary transistor in the cascode. An optimum sizing for the cascoded device was obtained through minimization of noise figure. Finally, an alternative design methodology based on the constant available gain method has been presented.

CHAPTER 3
CMOS LNA IMPLEMENTATION AND MEASUREMENTS

3.1 Overview

The previous chapter presented common-gate and source-degenerated LNAs which can achieve high gain, low noise figure, and low power consumption. Also, a detailed design methodology for source-degenerated LNAs was presented, considering gain, NF, input matching, and output matching. Methodologies, however, are only as good as their demonstrations; therefore, this chapter presents the implementation of CMOS LNAs, including design of passive components. Low noise amplifiers operating at 0.9, 8, 14, and 24 GHz are presented. The LNAs are implemented in 0.8-, 0.25-, 0.18-, and 0.10-μm CMOS technologies, respectively.

3.2 Passive Components

3.2.1 Inductor Design Techniques

The quality factor of the on-chip spiral inductors directly affects both LNA gain and noise figure. As already discussed, Q_{Ld} should be maximized to improve gain while decreasing power consumption. Although the series resistance of L_g was not included in (2.44), it can easily be shown that the series resistance of L_g (r_{Lg}) increases F by the quantity r_{Lg}/R_S. For these reasons, high quality-factor inductors are required for L_g and L_d. Depending on the inductance and the operating frequency, it may not be practical to integrate L_g, which is the case for a 900-MHz LNA.

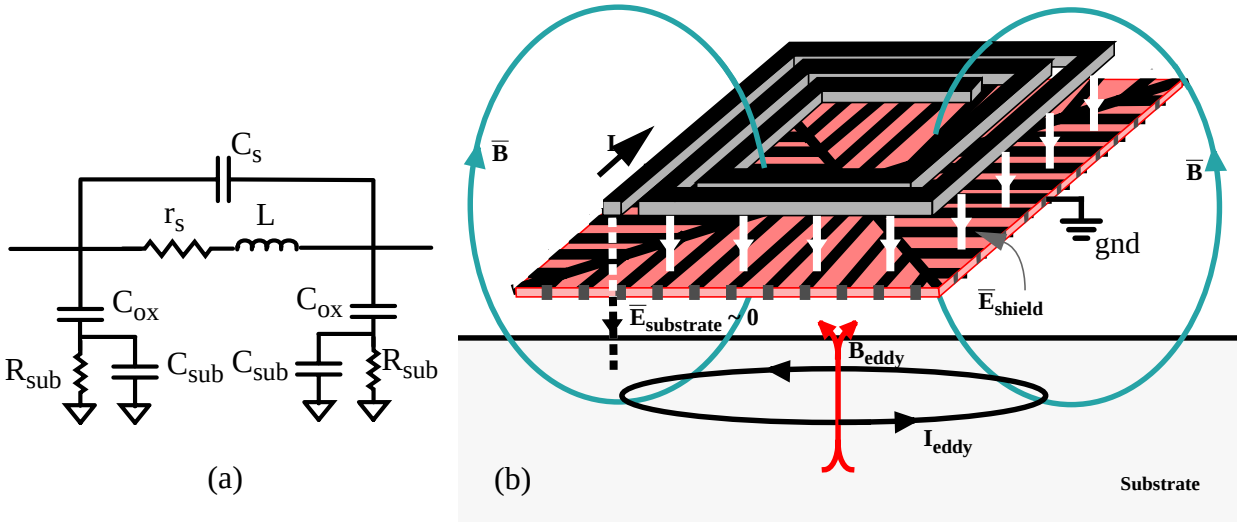


Figure 3-1 (a) General two-port lumped-element model for spiral inductor. (b) Illustration of a spiral inductor above a patterned-ground shield. The shield terminates most of $\overline{E}$-field while allowing $\overline{B}$-field to pass through, increasing Q.

A two-port lumped-element model for a general spiral inductor is shown in Figure 3-1(a). Using this model, the quality factor (Q) for an inductor with one port shorted to ground can be written as follows [Lon97], where substrate capacitance (C_{sub}) and port-to-port capacitance (C_s) have been neglected:

$$Q \approx \left(\frac{\omega L}{r_s}\right)\left(1 + \frac{\omega^4 L^2 C_{ox}^2 R_{sub}/r_s}{1 + \omega^2 C_{ox}^2 R_{sub}^2}\right)^{-1}. \qquad (3.1)$$

This accounts for loss in both the series resistance of the spiral and in the conductive silicon substrate. Note that the interaction of the substrate with the magnetic field is not captured with this equation (i.e., eddy-current effects). To maximize Q, the series resistance (r_s) should be minimized, oxide capacitance (C_{ox}) should be minimized, and *the substrate resistance (R_{sub}) should either be very small or very large*. This trend for R_{sub} is the same as that seen in the noise-figure analysis. In fact, this is a general trend which can be applied to any RF circuit or component [Flo00b].

One way to minimize the substrate resistance of the inductor is to use patterned ground shields [Yue98, Che98]. Referring to Figure 3-1(b), ground shields provide a low-resistance path to ground for capacitively coupled currents through termination of the $\overline{E}$-field. This reduces R_{sub} to approximately 5-10 Ω, and virtually eliminates C_{sub}. The shield is patterned to prevent eddy currents from flowing in the shield by not terminating the $\overline{B}$-field, which would decrease L and increase r_s. Instead, the eddy currents are forced into the substrate, with the magnitude of these currents being inversely proportional to the substrate resistivity [Flo00b]. In the commonly used substrate resistivity range, the substrate loss increases with decreasing resistivity. This effect shows up as an increase in the series resistance (r_s) in the inductor model. This effect is reduced for smaller-area inductors, since the magnetic field does not penetrate as deeply into the substrate, thereby reducing the eddy currents. The net result is an increase in inductor quality factor at the cost of increased parasitic capacitance or decreased self-resonant frequency.

3.2.2 Capacitor implementation

Capacitors C_1 and C_2 in Figure 2-2, as well as the bypass capacitors for bias voltages are implemented using accumulation-mode MOS capacitors [Hun98]. These capacitors achieve high Q-factors, and are compatible with standard digital CMOS technologies. The output dc voltage across C_1 is 0 V, consistent with driving an image-rejection filter. A concern with using this capacitor structure is the voltage-dependent capacitance and its effect on P_{1dB} and IP3 performance. However, measurements show that P_{1dB} and IP3 vary by less than 0.5 dB for the output dc voltage ranging from ground to V_{dd}.

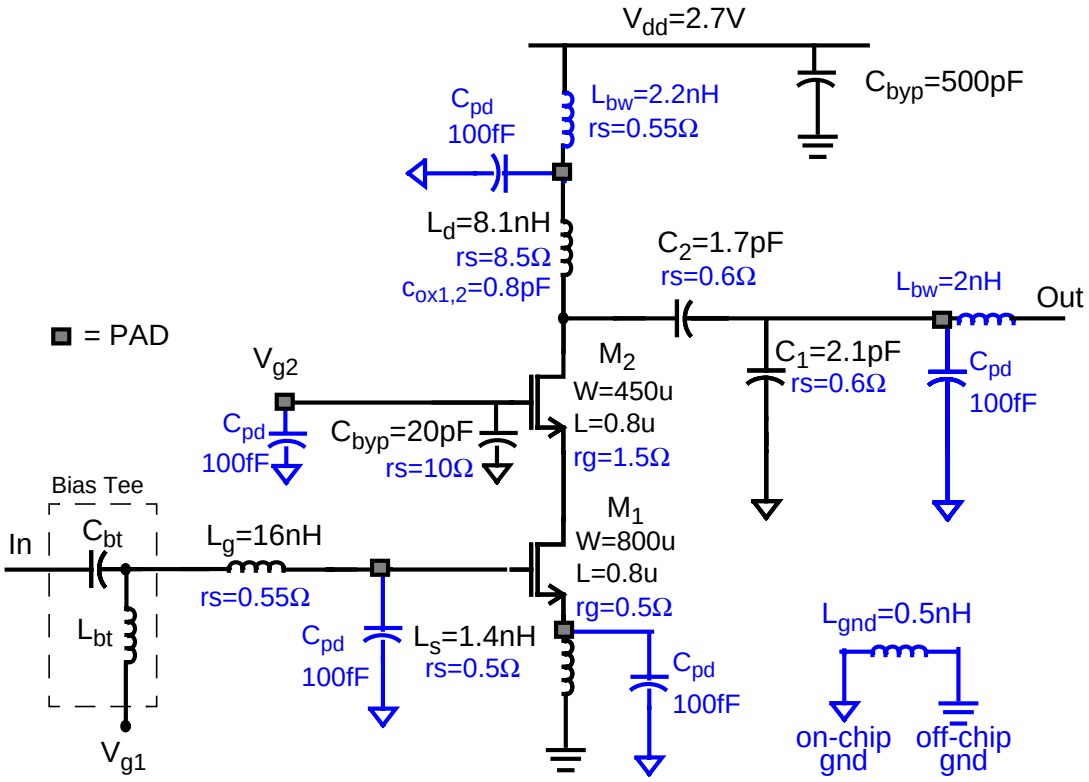
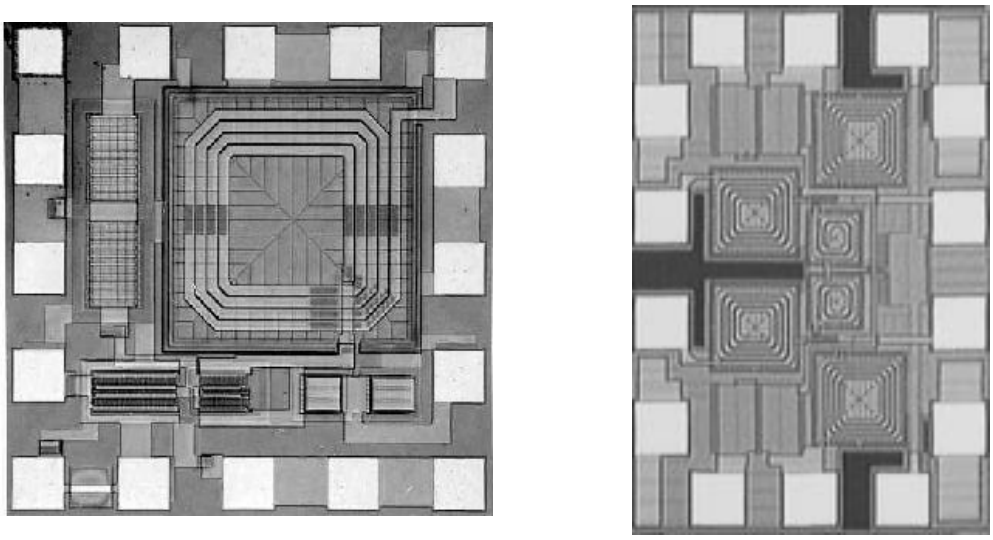


Figure 3-2 Schematic of 900-MHz source-degenerated CMOS LNA including on-chip and package parasitics.

3.3 A 900-MHz, 0.8-µm CMOS LNA

3.3.1 Circuit Implementation

To verify the design methodology for CMOS source-degenerated LNAs, a 900-MHz version was implemented in a 0.8-µm CMOS technology with 3 metal layers. This technology was obtained through MOSIS. Figure 3-2 shows the schematic of the LNA. The important on-chip and package parasitics are shown, including series resistances for inductors and capacitors (rs), pad capacitance (C_{pd}), gate resistance (rg), inductor parasitic capacitance (c_{ox}), and bondwire/ground inductance (L_{bw}/L_{gnd}). Both bias voltages, V_{g1} and V_{g2}, are generated off chip for flexibility in testing. Figure 3-3(a) shows a die photograph of the 900-MHz LNA [Flo99a]. The circuit area is 720x720 µm^2. This



(a) (b)

Figure 3-3 Die photographs of (a) 0.8-µm, 900-MHz single-ended CMOS LNA and (b) 0.25-µm, 8-GHz differential CMOS LNA.

LNA was packaged, therefore gold bond-wires are used to implement L_s as well as to improve the quality factor of L_d. The on-chip portion of L_d consisted of a ground-shielded, 4.25-turn, 8-nH spiral inductor with a quality factor of 4.5 at 900 MHz. It was implemented using metals 2 and 3 shunted together. The bondwire and pin added an additional 2.2 nH to L_d. For this operating frequency and technology, L_s is ~1.4 nH. An off-chip inductor is used for L_g, while an off-chip bypassing capacitor is required for V_{dd}. Finally, ground-shielded pads [Col98] are used to minimize the substrate resistance, improve the noise figure and reverse isolation, and control the pad impedance.

The 900-MHz LNA was packaged in an SOIC-like test package with low ground inductance, and mounted on a multilayer board. A parasitic inductance therefore exists between the on-chip ground and the board-level ground. If this inductance is too large, the reverse isolation is greatly reduced, due to feedback [Col98]. To minimize the ground inductance, 11 ground pads are included on chip and down-bonds from the on-chip ground to the paddle of the package are used, reducing the inductance to less than 0.4 nH. The paddle is then directly soldered to the board ground.

3.3.2 Measured Results

The LNA was characterized at four different operating points to study the trade-off between power consumption and NF. Figure 3-4(a) shows a plot of measured gain and NF versus bias current. Operating points 1 to 4 correspond to minimum to maximum NF and maximum to minimum power, respectively. At 10 mA of current (operating point 1), the LNA achieves a NF of 1.2 dB, which is competitive with most GaAs and bipolar LNAs. However, the power consumption is 30 mW, which is quite large. As the power consumption is decreased to 8.1 mW (operating point 3), the NF only increases to 1.78 dB. This result meets both of the desired performance metrics for CMOS LNAs (NF < 2 dB, and power < 10 mW). Measurements show that to achieve a NF of 2 dB, only 6.3 mW is required. Operating points 3 and 4 have comparable NF's to [Stu98] and [Hua98], but at only a fraction of their power. Much of this power savings comes from the ability to drive

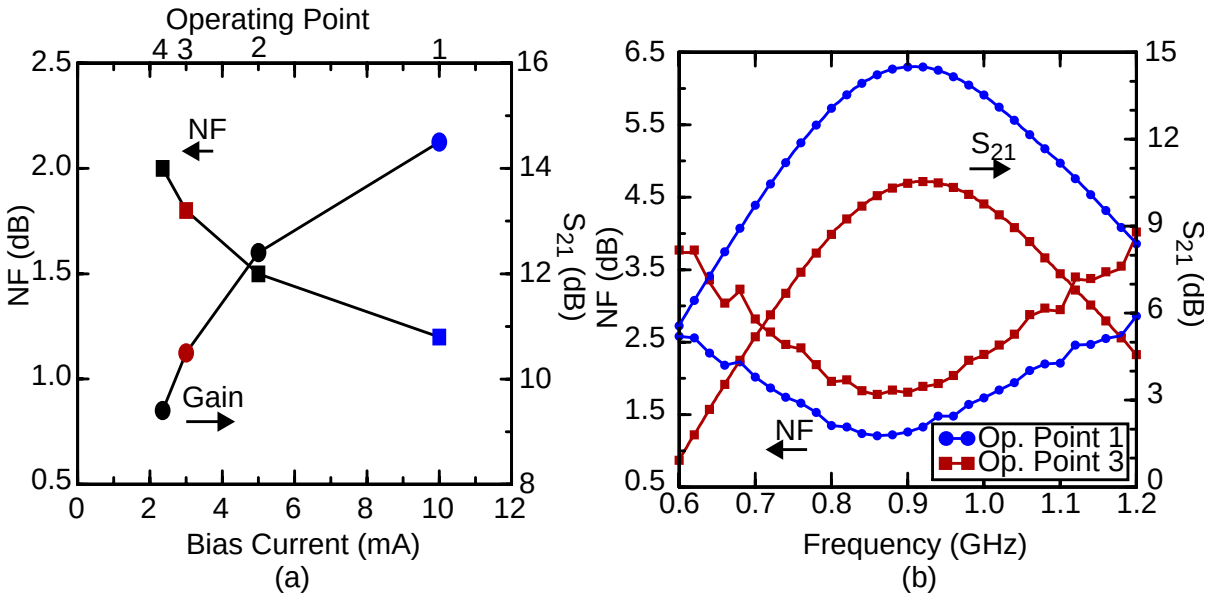


Figure 3-4 (a) Measured gain (S_{21}) and noise figure (NF) versus bias current. Four different operating points are shown, numbered 1 to 4, corresponding to minimum to maximum NF and maximum to minimum current, respectively. (b) Gain and NF versus frequency for operating points 1 & 3.

50 Ω without an additional output buffer. Figure 3-4(b) shows a plot of the transducer gain (S_{21}) and NF versus frequency for the LNA, for operating points 1 and 3. At 900 MHz, the measured transducer gains (S_{21}) are 14.5 and 10.5 dB at 30 and 8.1 mW, respectively.

Figures 3-5 (a) and (b) show the input and output reflection coefficients (S_{11} and S_{22}) for operating points 1 and 3. The relatively high S_{11}'s are due to the bond-wire inductance being too small, generating only ~15 Ω of real impedance. To improve the input match to under -10 dB, L_s should be slightly increased while L_g can be decreased to maintain the noise match. S_{22} is below -10 dB over a 137-MHz span. The very low S_{22} corresponds to a conjugate match at the output.

To measure F_{min}, the measurement setup shown in Figure 3-6(a) was used. External tuners are inserted at the input and output of the packaged LNA, and the impedances of these tuners are adjusted until the optimum noise matching condition (i.e., Γ_{opt} or Z_{opt}) occurs, corresponding to F_{min}. Figure 3-6(b) shows the optimum source-reflection coefficient (Γ_{opt}) versus frequency for operating points 1 and 3, plotted on Smith charts. Figure

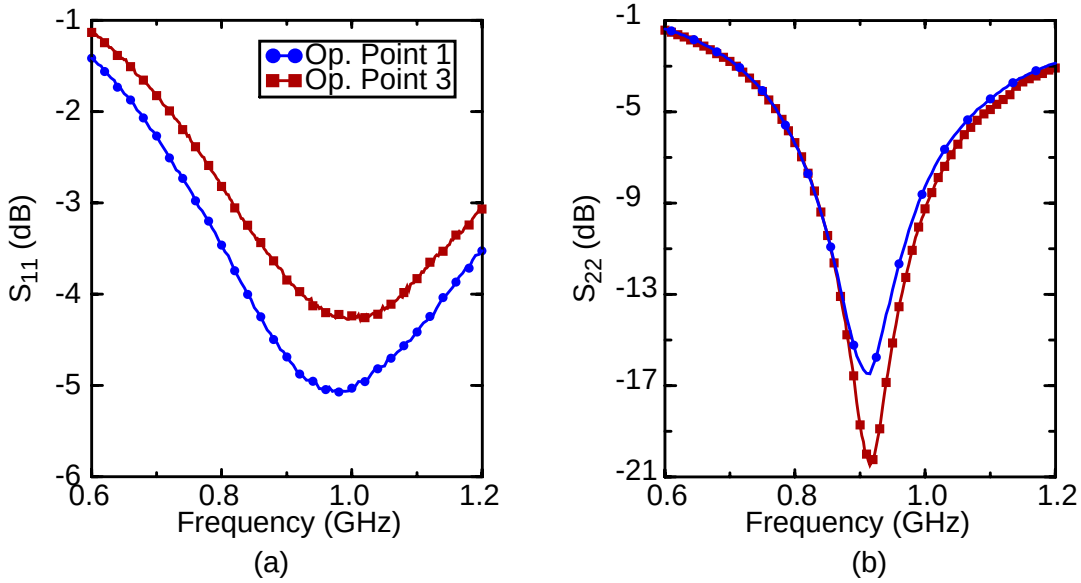


Figure 3-5 (a) Input (S_{11}) and (b) Output (S_{22}) reflection coefficients versus frequency, operating points 1 and 3.

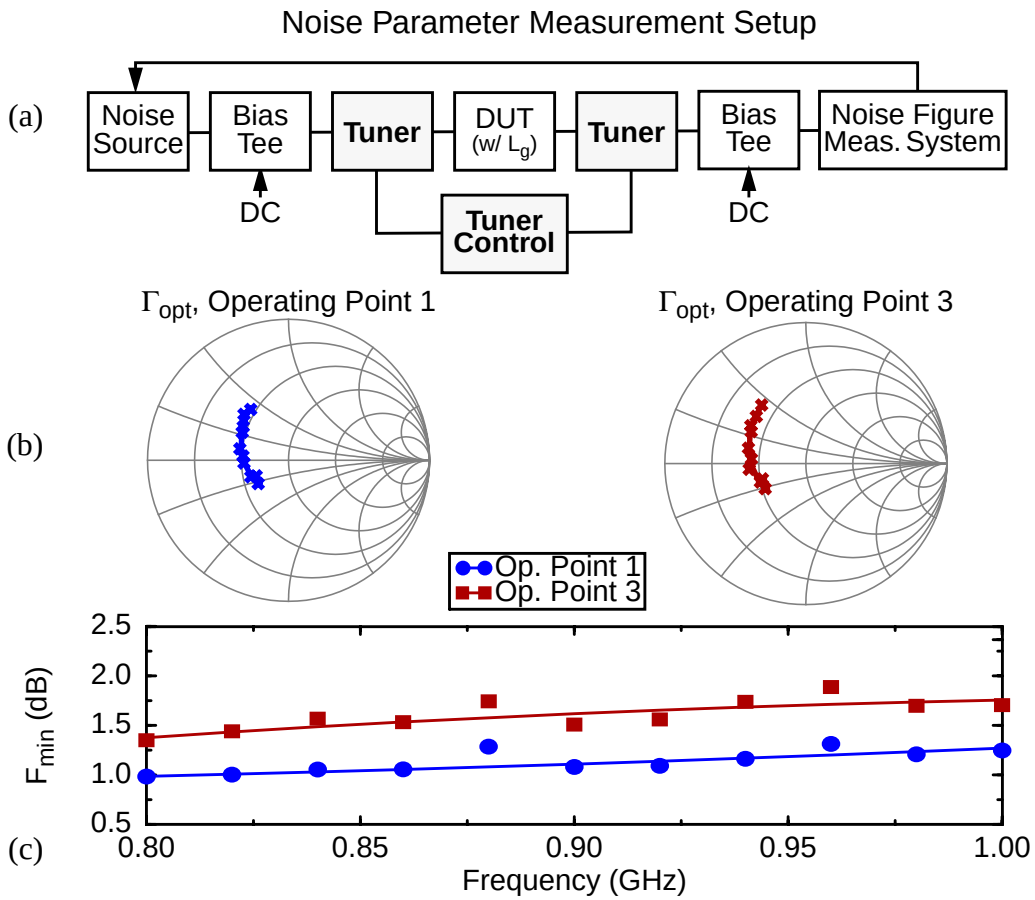


Figure 3-6 (a) Measurement system used to obtain F_{min} and Γ_{opt}.
(b) Optimum source reflection coefficient for minimum noise (Γ_{opt}).
(c) Minimum noise figure versus frequency.

Table 3-1 Measured noise parameters at 900 MHz for 0.8-µm CMOS LNA

Operating Point	Current (mA)	F_{min} (dB)	Γ_{opt}	$F(S_{11} = -\infty$ dB) (dB)	$F(S_{11}$=-10dB) (dB)
1	10	1.08	$0.355\angle 166^o$	1.46	1.12
2	5	1.32	$0.395\angle 167^o$	1.79	1.38
3	3	1.51	$0.421\angle 165^o$	2.02	1.56
4	2.35	1.66	$0.434\angle 163^o$	2.18	1.72

3-6(c) shows the measured F_{min} versus frequency for operating points 1 and 3, along with a curve fit to the measured data. Table 3-1 shows the measured noise parameters (excluding R_n) for each operating point. At 900 MHz, F_{min} is 1.08 and 1.51 dB, for operating

points 1 and 3, respectively. To match the input to obtain F_{min}, L_g should be increased and an off-chip capacitor should be added. This transforms the 50-Ω source impedance to Z_{opt} (equivalent to reflection coefficient Γ_{opt}). However, Γ_{opt} for the LNA is not equal to S_{11}^*, therefore the noise matching condition and the power matching condition do not coincide. Table 3-1 also shows the NF corresponding to perfect input power matching (i.e., S_{11} = -∞ dB). The noise parameters can therefore be used to derive the optimal input matching network, such that minimum noise figure is obtained while S_{11} is constrained to be -10 dB. As shown in Table 3-1, these noise figures are 1.12 and 1.56 dB for operating points 1 and 3, which are very close to their respective F_{min}. To obtain these NF at S_{11}=-10 dB, L_g should be increased by 4 nH and a 4-pF shunt capacitor should be added to the LNA input.

The reverse isolation for each operating point is very good with more than 42 dB of isolation for each bias condition. As mentioned earlier, this is due to the use of a package with low ground-inductance, ground-shielded pad structures, a ground-shielded inductor, and a cascode amplifier. The measured P_{1dB} and IP3 data for each operating point are shown in Figure 3-7. As can be seen, the power of the intermodulation product (P_{2f1-f2}) is unchanged by the current level in the LNA. However, the output power of the fundamental (P_{f1}) depends on the operating power gain at the specific current level. Therefore, the IIP3 relatively scales in accordance with the gain. The output power level at which the LNA compresses is a function of the supply voltage, which is 2.7 V for operating points 2-4 and 3 V for operating point 1. Therefore, the P_{1dB} (output) is approximately the same for each operating point, while P_{1dB} (input) scales with the gain. The measured IIP3's at 30 mW and 6.3 mW are -1 dBm and -3.8 dBm. Due to the use of a single-stage topology, the amplifier is very linear, and is suitable for GSM applications.

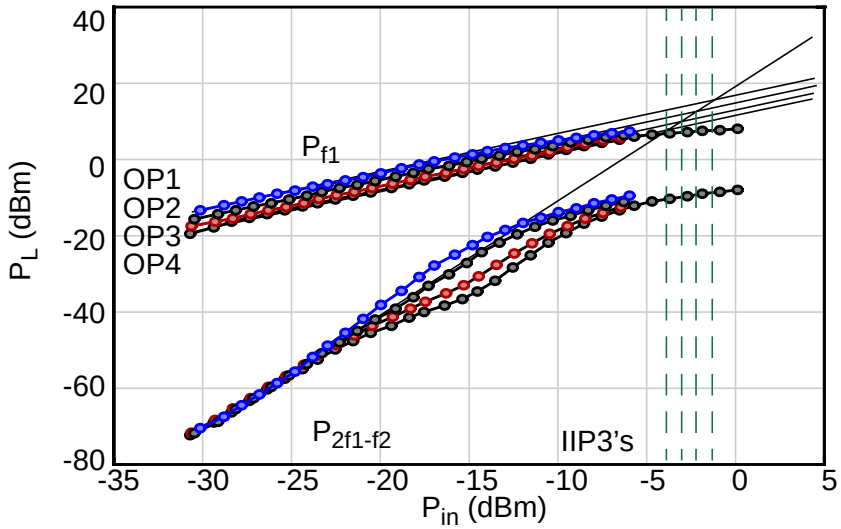


Figure 3-7 Measured P_{1dB} and IIP3, operating points 1-4.

Table 3-2 Summary of measured characteristics for 900-MHz CMOS LNA

f_0 = 900 MHz	Op. Point 1	Op. Point 2	Op. Point 3	Op. Point 4
Power (mW)	30	13.5	8.1	6.3
Gain (dB)	14.5	12.4	10.5	9.4
50-Ω Noise Figure (dB)	1.2	1.5	1.8	2.0
F_{min} (dB)	1.08	1.32	1.51	1.66
F (S_{11}=-10 dB) (dB)	1.12	1.38	1.56	1.73
V_{DD} (V)	3.0	2.7	2.7	2.7
S_{11} (dB)	-4.7	-4.1	-3.9	-3.8
S_{22} (dB)	-15.9	-16.7	-16.9	-17.0
S_{12} (dB)	< -42	< -42	< -42	< -42
IIP3 (dBm)	-1	-1.9	-3.3	-3.8
P_{1dB} (input) (dBm)	-12.4	-10.4	-6.3	-3.8

3.3.3 Summary for 900-MHz LNA

A summary of the measured characteristics for each operating point is shown in Table 3-2. Operating point 1 has an F_{min} which is 0.08 dB higher than a 900-MHz CMOS

LNA implemented in a 6-level-metal 0.35-μm BiCMOS process [Gra00], which is currently the lowest NF for any CMOS LNA. However, considering that [Gra00] employs technology two generations beyond 0.8-μm, with an ω_T approximately five times as large, and that the back-end metal process and substrate in [Gra00] allow for inductor quality factors approximately 3 times as large as the 0.8-μm process, the result achieved in this work is excellent. Also, the performance goals of NF < 2 dB and power < 10 mW have been achieved, demonstrating the competitiveness of CMOS for wireless applications. Finally, the LNA exhibits excellent linearity and is suitable for wireless applications.

3.4 An 8-GHz, 0.25-μm CMOS LNA

3.4.1 Circuit Implementation

Having demonstrated the design methodology for source-degenerated CMOS LNAs at 900 MHz, both a single-ended and differential version of the source-degenerated LNA was implemented in a standard 0.25-μm CMOS technology, operating at ~8 GHz. This LNA was also implemented with an entire clock receiver, as will be presented in Chapter 6. The technology provides 5 metal layers, and both p^- (~8 Ω-cm) and p^+ with epitaxial layer (~0.01 Ω-cm) substrates, allowing the effects of substrate resistivity on LNA performance to be studied. This technology was obtained once again through MOSIS.

Figure 3-3(b) shows a die photograph of the 8-GHz differential LNA, while Figure 3-8 shows a schematic of the differential LNA, including important parasitics (pad capacitances are implied for each labelled input). The die size is 730x510 μm^2. All three inductors, L_d, L_g, and L_s are integrated, as well as 20-pF bypass capacitors. Symmetry was maintained top-to-bottom for the differential layout to avoid any systematic errors from layout mismatch. Again, ground-shielded pads are used throughout the layout.

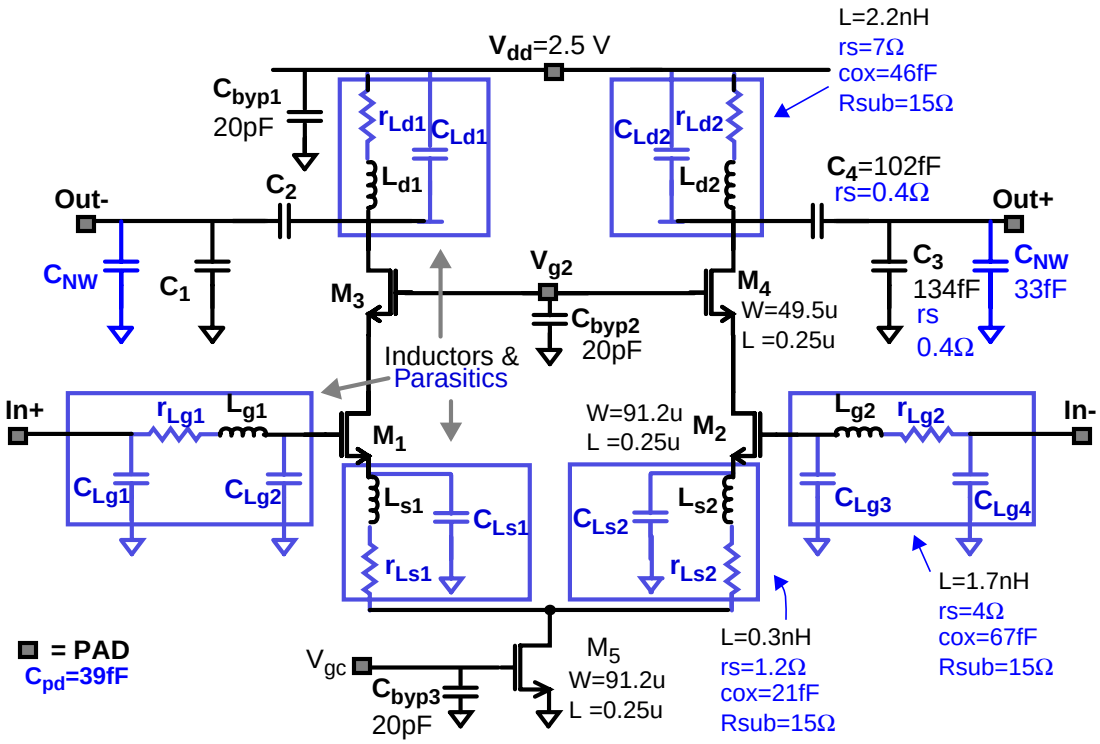


Figure 3-8 Schematic of 8-GHz fully differential LNA showing parasitics.

This LNA is a fully differential version of that given in Figure 2-2. As mentioned in the first chapter, a differential topology is required for the clock receiver application. Transistor M_5 provides tail current to the differential amplifier, where V_{bias} is externally generated. An important difference between this LNA and the 900-MHz LNA, is that inductors $L_{g1,2}$ and $L_{s1,2}$ are integrated. This LNA was originally designed to provide 12.6 dB of gain while driving 50 Ω, and the anticipated NF was approximately 3 dB. The higher anticipated NF, compared to the 900-MHz result, is due to short-channel effects increasing γ [Jin85], as well as the integration of L_g. According to simulations, the integration of L_g increases the NF by approximately 0.6 dB. First, the increase is due to thermal noise generated by the series resistance of L_g (r_{Lgi}), whose Q factor is 10 (5) for p^- (p^+) substrates. Second, the parasitic capacitances at the input and output ports of L_g (C_{Lgi}) move the input match away from the optimal noise match. Therefore, the integration of L_g

imposes severe restrictions on the achievable noise figure. For standard wireless applications at this frequency range, L_g is approximately 2 nH, which is suitable for bondwire implementation. This would increase the Q dramatically and help the noise figure. However, for the wireless interconnect application, since the antenna is integrated, L_g has to be integrated as well.

3.4.2 Inductor Characteristics

To demonstrate the effect of substrate resistance on inductor quality factor, 1.8-nH spiral inductors have been implemented in the 5-level-metal, 0.25-μm CMOS process on both p^- and p^+ (with epitaxial layer) substrates. These inductors were used for L_g in the LNA. The inductor is implemented using shunted metals 3, 4, and 5 layers with 2.5 turns and an area of 100x100 μm^2. The quality factor is estimated using both the half-bandwidth method [O98] and the conventional method (Q_{11}=-imag(y_{11})/real(y_{11})). Figure 3-9 shows

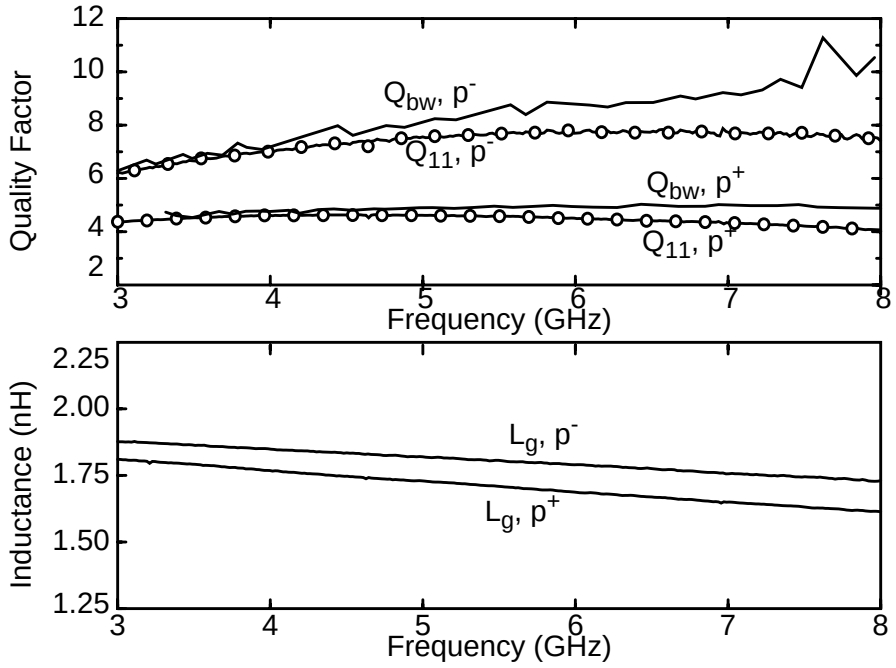


Figure 3-9 Quality factors and inductance of L_g versus frequency for different substrate resistivities (p^+ ~ 0.01 Ω-cm, p^- with epi ~ 8 Ω-cm). The inductor is implemented in a 5-metal-layer 0.25-μm CMOS process.

the measured Q and inductance of these inductors for both substrate types. The quality factor of the inductor on p^+ substrates (Q=5) is ~50% of that on p^- substrates (Q=10). For p^+ substrates, the inductance slightly decreases, while the series resistance nearly doubles, due to the induced eddy currents. Measurements also show that for a 1-nH inductor with an area of 90x90 μm^2, the Q reduction is only ~30% [Flo00b]. This signifies that smaller area inductors are beneficial for low-resistivity substrates.

3.4.3 Measured Results

Figure 3-10(a) shows the measured S-parameters for the differential LNA. To obtain this balanced measurement using an unbalanced network analyzer, 180^o couplers were placed at the input and output of the LNA, acting as baluns. Driving 100 Ω differentially, the LNA provides 10 dB of gain, with input and output reflection coefficients of less than -15 dB, consuming 21 mW from a 2.5-V supply. This gain is ~ 3 dB lower than that expected, due to a discrepancy between the simulated transistor characteristics and the measured transistor characteristics. In particular, C_{gs} was 80% larger than that simulated; thus, ω_T was lower and the gain was decreased, as given by (2.26).

Figure 3-10(b) shows the measured gain and NF of the single-ended LNA for both p^- and p^+ substrates. Each LNA consumes 10 mW from a 2.5-V supply. The power gain of the LNA on a p^- substrate is ~7.3 dB, while that for the LNA on a p^+ substrate is ~1 dB. For the p^- substrate, there is a 2.7-dB difference between the gain for the single-ended and differential LNAs, whose origin is unknown. Theoretically, the gains should be the same when each half-circuit of the differential LNA is operated at the same power consumption as the single-ended LNA. Referring to Figure 3-9, the spiral inductor Q for p^+ substrate is

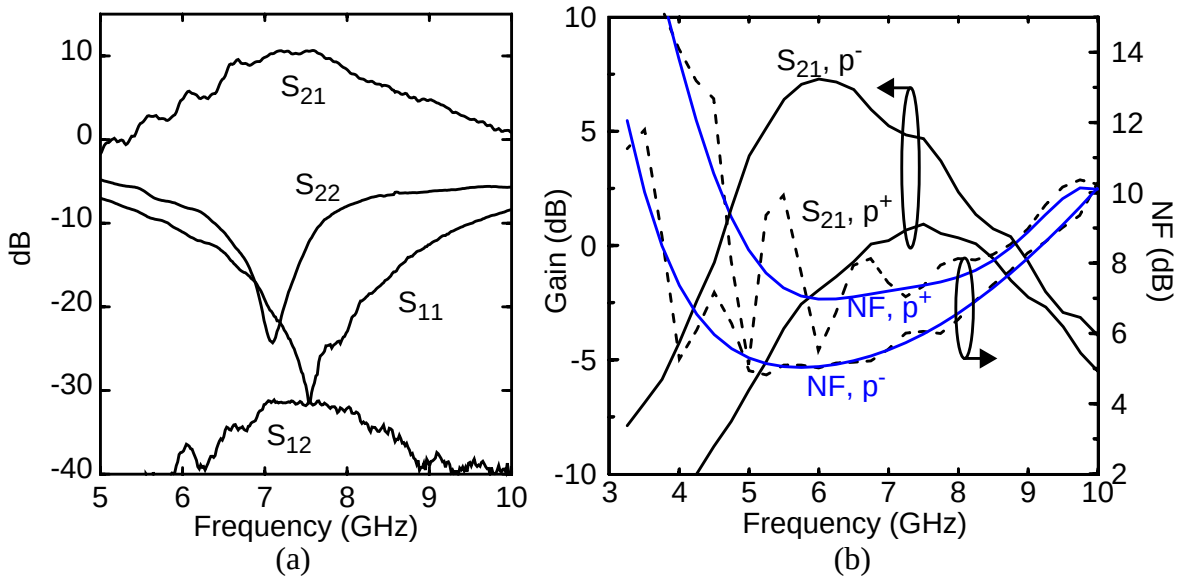


Figure 3-10 (a) Measured S-parameters of differential LNA. (b) Measured gain and NF for single-ended NF for both p^+ and p^- substrates.

~50% of that for p^- substrate, and the inductance is smaller. Therefore, the resonant frequency of the p^+ LNA is about 25% higher due to the decreased inductance. Simulation results show that ~4 dB of the gain reduction can be attributed to the 50% reduction in the Q for L_d. Another ~1 dB comes from the additional loss due to the increase in r_{Lg}.

The NF of the single-ended p^+ LNA is ~7.4 dB, which is 2.5 dB higher than the noise figure for the p^- LNA. The increased NF is partly attributed to the increased thermal noise generated by the series resistance of the inductors. However, a large part of the increased NF is due to the decreased gain, resulting in higher input-referred noise from output noise components. Although the substrate resistance is higher for p^-, the use of multiple-fingered transistors with many substrate contacts helps to mitigate its effect on NF. These results reveal the benefits of high-resistivity substrates for RF applications.

Table 3-3 Summary of measured results for 8-GHz, 0.25-µm LNAs.

Differential LNA (p^- substrate)		Single-Ended LNAs	
V_{dd}	2.5 V	V_{dd}	2.5 V
Power Consumption	21 mW	Power Consumption	10 mW
Resonant Frequency	7.4 GHz	Res. Frequency (p^- substrate)	6 GHz
Gain	10 dB	Gain (p^- substrate)	7.3 dB
S_{11}	-26 dB	NF (p^- substrate)	4.9 dB
S_{22}	-15.5 dB	Res. Frequency (p^+ substrate)	7.5 GHz
Reverse Isolation	32 dB	Gain (p^+ substrate)	1 dB
		NF (p^+ substrate)	7.4 dB

3.5 A 14-GHz, 0.18-µm CMOS LNA

3.5.1 Circuit Implementation

A final implementation of a source-degenerated LNA was done in a 0.18-µm CMOS technology with 6 layers of copper interconnects [Flo01a]. This technology was obtained from UMC as part of the SRC Copper Design Challenge, sponsored by the Semiconductor Research Corporation (SRC), Novellus, SpeedFam-IPEC, and UMC. The substrate resistivity is 15-25 Ω-cm. The circuits were designed to operate at ~21 GHz, while measurements reveal ~14 GHz operation.

For this technology, both a single-stage differential LNA and an LNA with source-follower buffers were implemented. The operation of source-followers will be presented in section 3.6. The schematic of the single-stage LNA is identical to the 8-GHz version shown in Figure 3-8, where component values and sizes were modified, as reflected in Figure 3-11. Figure 3-12 shows a schematic of the fully differential LNA with

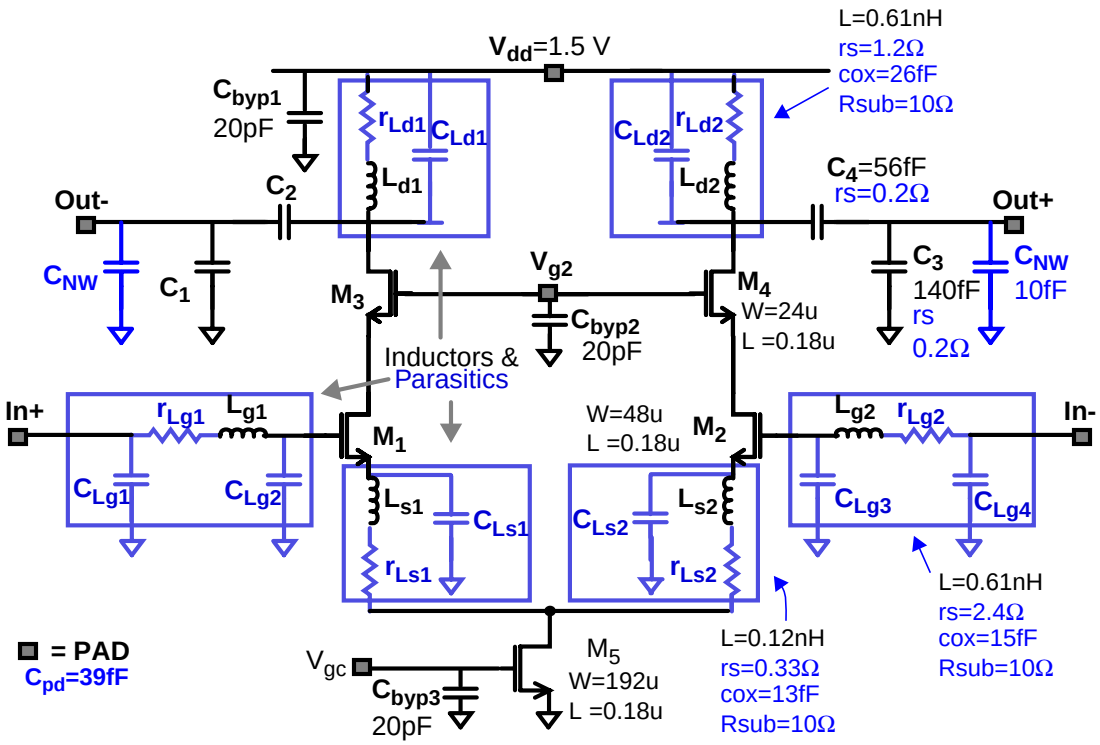


Figure 3-11 Schematic of 14-GHz fully differential LNA showing parasitics.

source-follower buffers. This circuit is used in the clock receiver, driving the frequency divider. Two different input matching conditions were implemented. The input matching condition was 100 Ω (differentially) when the LNA was measured using 50-Ω test equipment, and 125-j55 Ω when the LNA was driven by the on-chip antenna. Therefore, the reactance of the gate inductors for the latter case was increased by 27 Ω (each side or 55 Ω differentially). The single-stage differential LNA was differentially matched at the output to 100 Ω, using capacitive transformers. Figure 3-13(a) shows a die photograph of the 0.18-μm differential LNA. The die size is 745x410 μm^2.

3.5.2 Inductor Characteristics

The gate and drain inductors for the 14-GHz LNA have the following design parameters: inductance = 0.6 nH, turns = 2.5, area = 67x67 μm^2, width = 5-μm, and turn

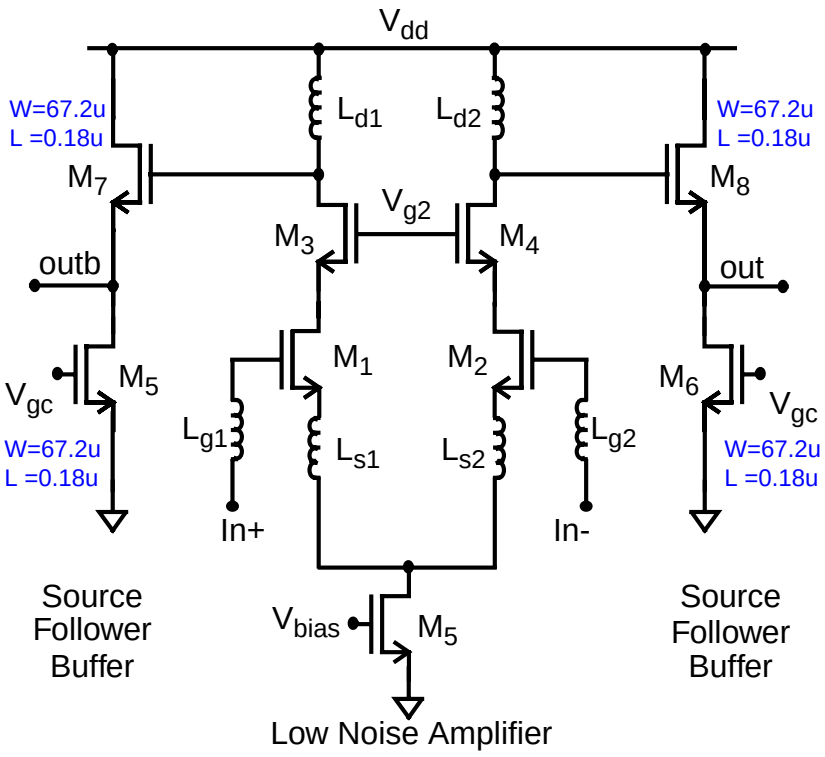
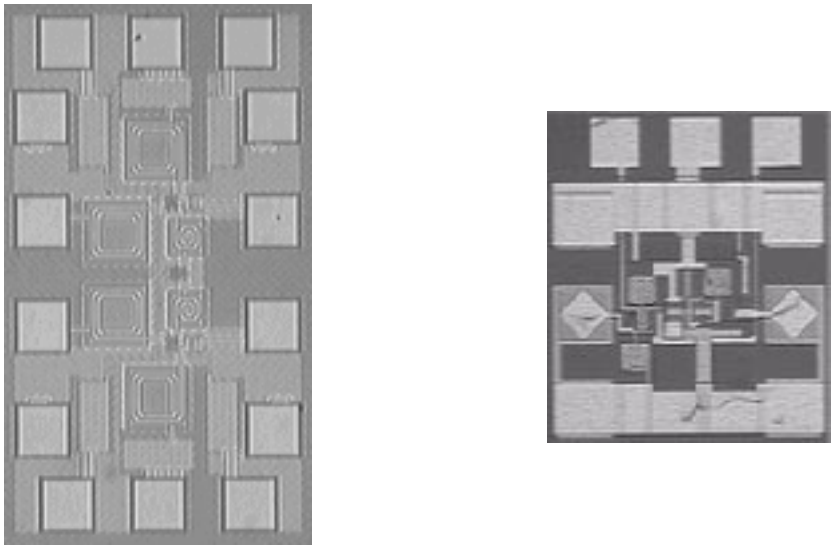


Figure 3-12 Schematic of differential 14-GHz LNA with source-followers.



(a) (b)

Figure 3-13 Die photographs of (a) 0.18-µm, 14-GHz differential CMOS LNA and (b) 0.1-µm, 23.8-GHz SOI CMOS tuned amplifier.

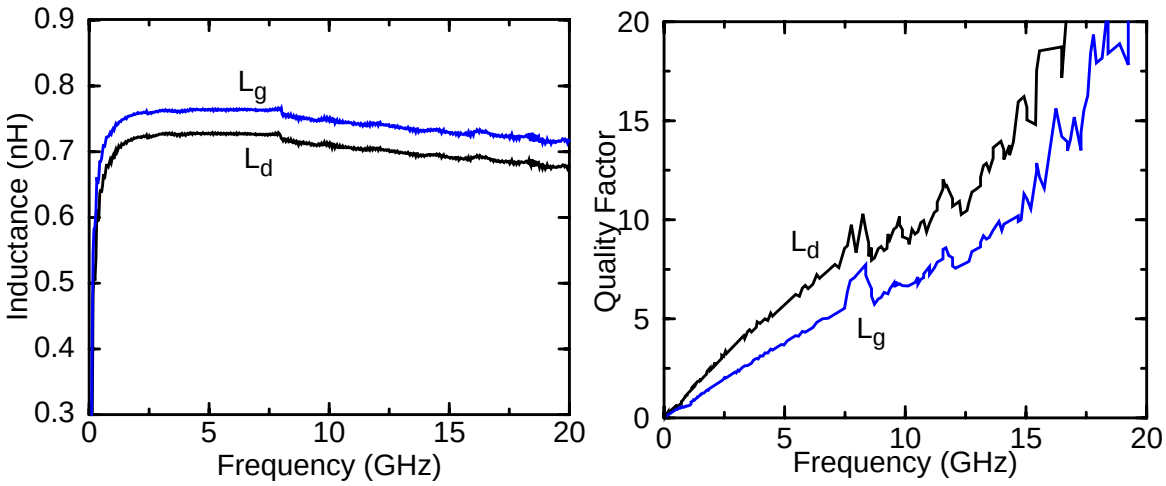


Figure 3-14 Measured (a) inductance and (b) quality factor (Q_{bw}) for L_g, and L_d.

spacing = 1.25-μm. Patterned-ground shields were again used to decrease the substrate resistance. Since this technology has a high-resistivity substrate, the increase in series resistance, and hence degradation in Q, caused by eddy currents in the substrate is small, as was shown in section 3.4.2. L_d was implemented using metals 5 and 6 shunted together, decreasing the series resistance and maximizing Q. Simulations show that for L_g, minimizing the parasitic capacitance has a greater effect on NF than minimizing the series resistance (provided the Q is > 20). This is due to the capacitance moving the input matching condition away from the optimum noise match. Therefore, due to the availability of copper, only metal 6 was used for L_g.

A key benefit of copper metallization is its reduction of interconnect series resistance. For inductors, the Q will be almost doubled as compared with the same-thickness aluminum (equal to the ratio of the Al and Cu resistivities). Both metals 5 and 6 were to have a nominal thickness of 1 μm. However, during fabrication these two metal layers had to be thinned from 1 μm to approximately 0.5 μm. Therefore, r_s was increased and Q was decreased. Figure 3-14 shows the measured inductance and quality factor (Q_{bw} [O98])

Table 3-4 Comparison Between Expected and Measured Inductor Characteristics

Inductor (15 GHz)		L (nH)	r_s (Ω)	C_{ox} (fF)	R_{sub} (Ω)	Q
L_{gate}	Expected	0.61	2.41	15.2	10	21.4
	Measured	0.73	6	26	~10	10.9
L_{drain}	Expected	0.61	1.2	25.9	10	28.6
	Measured	0.69	3.5	30	~10	15

versus frequency for L_g and L_d. The best Q is approximately 10 at 10 GHz, and increases to approximately 20 at 20 GHz. Table 3-4 shows a comparison between the expected and measured inductor characteristics. First, the measured inductance is ~0.1 nH larger than that expected, resulting in decreased circuit resonant frequency. Second, the measured series resistance is more than twice that expected, due to increased metal sheet resistance, while the measured Q is about half that expected.

Although the Q's are not as high as expected, they are certainly adequate for implementing RF circuitry, provided that the impact of lower Q is accounted for during the design phase. These results illustrate the dramatic effect that decreasing the top-level metal(s) sheet resistance has on inductor characteristics. Nevertheless, for constant metal thickness, copper metallization greatly improves inductor characteristics over aluminum metallization. Thus, these results are approximately twice as good as an all-aluminum process with the same metal thicknesses, or about comparable to an aluminum process with twice the metal thickness. These measurement results suggest that greatly improved inductor characteristics can be attained by thickening metal 5 and 6 layers.

3.5.3 Transistor Characterization

The 0.18-μm LNA and the entire wireless interconnect system were designed to operate at ~21 GHz. However, as will be shown in the subsequent sections, the operating frequency for these circuits has shifted down to ~14 GHz. Referring to Table 3-4, it can be seen that the measured inductance and its parasitic capacitance were slightly higher than expected (within 0.1 nH). At ~20 GHz, these discrepancies can account for at most a 3-GHz frequency shift. To understand the remaining frequency shift, the designs have been reviewed to make sure that all of the metal parasitics have been properly accounted, and that the transistors have been specified correctly including the area and perimeter of drains and sources. The remaining frequency shift is therefore believed to be primarily due to the differences between the CAD *intrinsic* transistor model used during the design process and the actual fabricated transistor characteristics. Note that the models used to design these RF circuits were the standard BSIM models, to which extrinsic parasitic components important at radio frequencies are added (e.g., R_{gate}, R_{sub}, and capacitances associated with interconnecting the multiple fingers of the transistor). This technique has been used very effectively in the past to yield simulated results which agree very closely with measured results.

The S-parameters of individual NMOS and PMOS transistors have been measured to quantify the difference in capacitance between the model and the actual transistors. Both the NMOS and PMOS transistors have W=18.8 μm and L=0.18 μm, and are implemented with 0.94-μm long fingers (total fingers = 20). The S-parameters of the transistors are then transformed into y-parameters. Parasitics associated with the pads are de-embedded through y-parameter subtraction of an open test structure. With the transis-

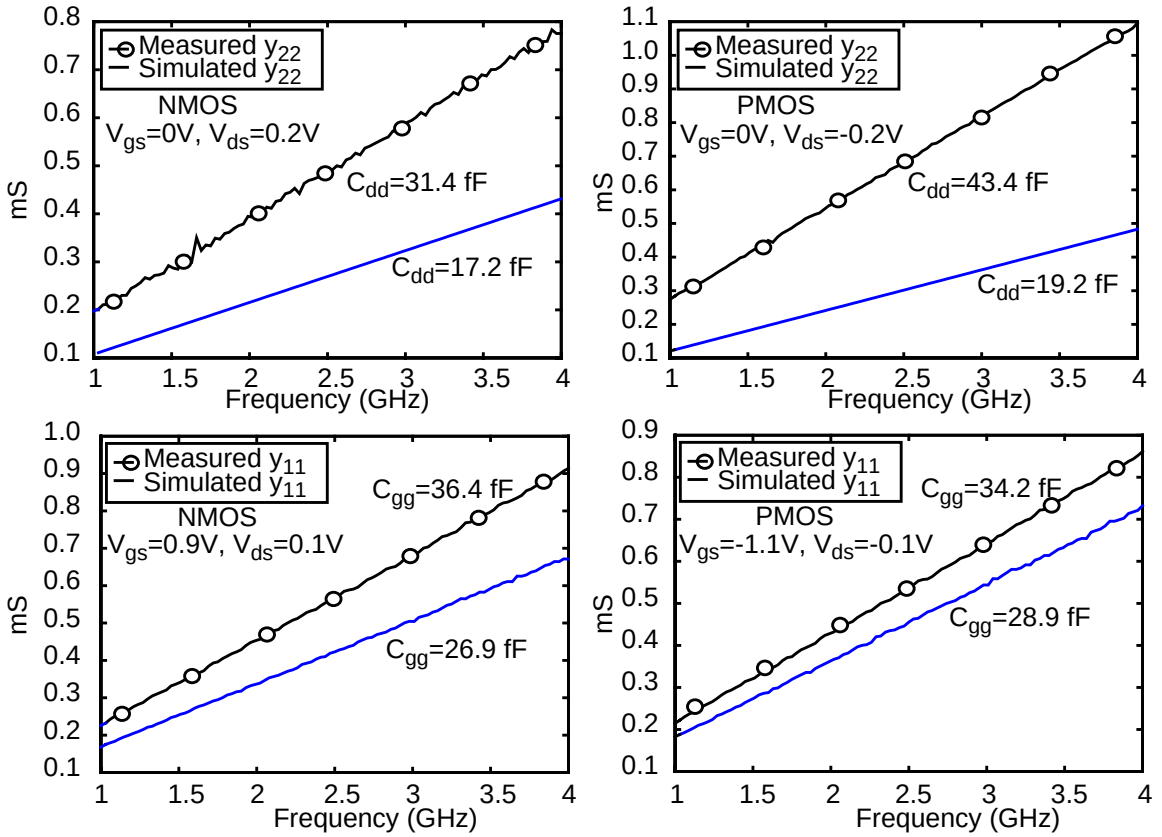


Figure 3-15 Measured versus simulated y_{11} (with transistor in linear region) and y_{22} (with transistor off) for NMOS and PMOS transistors. The slope of these lines over 2π is equal to the capacitances C_{gg} and C_{dd} for y_{11} and y_{22}, respectively.

tor biased in the linear region, y_{11} yields the total gate capacitance ($C_{gg} = C_{gs} + C_{gd} + C_{gb} \cong WLC_{ox} + 2WC_{ov}$). With the transistor turned off, the channel conductance is zero, and y_{22} yields the total drain capacitance ($C_{dd} = C_{db} + C_{gd}$), while y_{12} yields C_{gd}. Although there are more accurate ways to obtain these capacitances, this measurement provides a quick and easy way to observe any capacitance trends. Figure 3-15 shows the measured versus simulated y_{11} and y_{22} for the NMOS and PMOS transistors. The slope of each of these lines is proportional to capacitance, therefore the steeper the line, the higher the capacitance. As can be seen, the measured capacitances are all higher than the simulated capacitances (note--because the open pad structure used for de-embedding does not include the interconnects to the transistor, the measurements overestimate the capacitances

by a few fF). For NMOS, the gate capacitance is ~1.3 times larger, while for PMOS it is 1.2 times larger. For both NMOS and PMOS, the total drain capacitance is approximately twice that which is simulated, with the PMOS difference being more severe. This can result in as much as a 1.4 times ($\sqrt{2}$) reduction in resonant frequency for a tuned circuit.

3.5.4 Measured Results

Figure 3-16(a) shows the measured gain (S_{21}) and noise figure (NF) for the single-stage LNA matched to 100 Ω at the input and output, while Figure 3-16(b) shows the measured input and output reflection coefficients (S_{11} and S_{22}). Driving 100 Ω differentially, the LNA provides 8 dB of gain at 13.3 GHz, with S_{11} and S_{22} equal to -8 and -15 dB, respectively. The LNA consumes 12 mW from a 1.5-V supply. The reverse isolation is better than 27 dB. Finally, the 100-Ω noise figure is 7.7 dB at resonance. The results are summarized in Table 3-5.

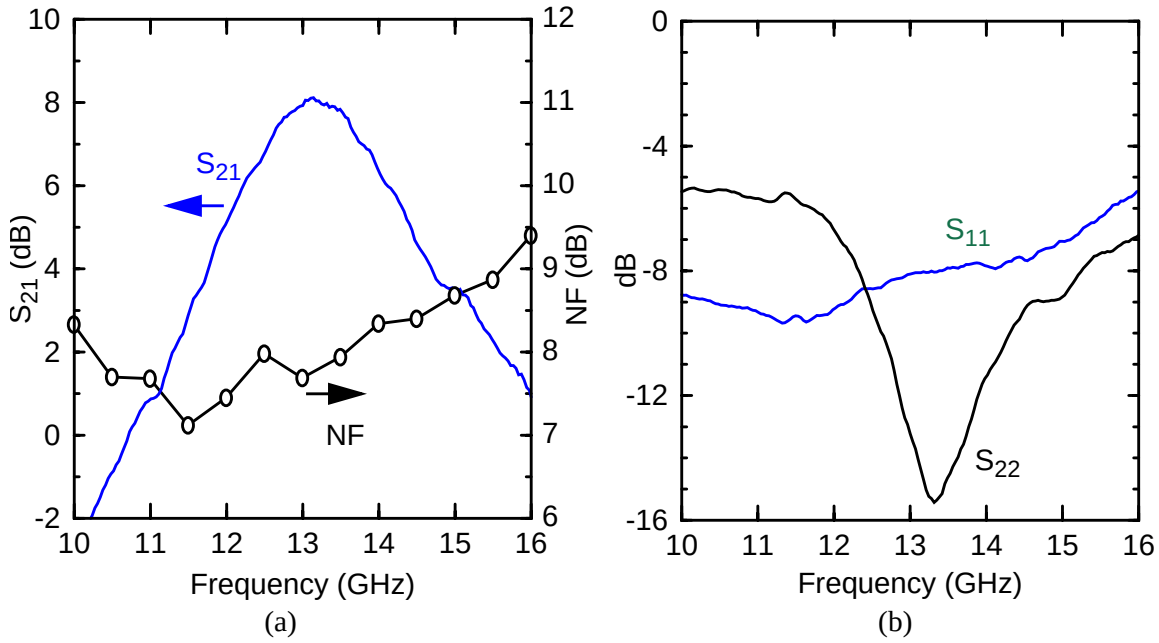


Figure 3-16 (a) Measured gain and noise figure for 0.18-µm LNA.
(b) Measured input and output reflection coefficients for 0.18-µm LNA.

Table 3-5 Summary of measured results for 14-GHz, 0.18-µm LNAs with copper.

Single-Stage Differential LNA		Differential LNA with Source-Followers	
Center Frequency	13.3 GHz	Center Frequency	14.4 GHz
Gain	8 dB	Gain at V_{gc}=0.5V	21 dB
S_{11}	-8 dB	Gain at V_{gc}=0.9V	25 dB
S_{22}	-15 dB	S_{11}	-5 dB
Reverse Isolation	27 dB	Reverse Isolation	32 dB
Noise Figure	7.7 dB	Noise Figure	8 dB
V_{dd}	1.5 V	V_{dd}	1.5 V
Power Consump-tion	12 mW	Power Consump-tion (V_{gc}=0.5V)	28.2 mW

Simulations predicted a 14-dB gain, a 3-dB NF, and a 21-GHz resonant frequency. The reduced resonant frequency has already been accounted for, due to the increased inductance and the larger transistor capacitances. Referring to equation (2.26), a 50% reduction in Q results in a 6-dB reduction in $|S_{21}|^2$. This accounts for the drop in S_{21} from the expected value of 14 dB to the measured value of 8 dB. The understanding of the higher noise figure is not as straight-forward, though. First, these noise measurements were obtained through on-wafer probing using external baluns, which yields higher noise figures (on the order of 1-2 dB) as compared to packaged chips, due to variations in the contact resistance of the probe. Second, generally speaking, as the gain is decreased, the noise figure increases, due to higher input-referred noise. Third, decreased inductor Q results in more thermal noise generated by the resistive loss of the inductors. This is particularly severe for L_g and L_s, which are located at the input of the LNA. Fourth, the modeling of the transistor's thermal noise coefficient (γ, which was assumed to be 1.17 in simulations based on 0.25-µm measurement results, is expected to increase with

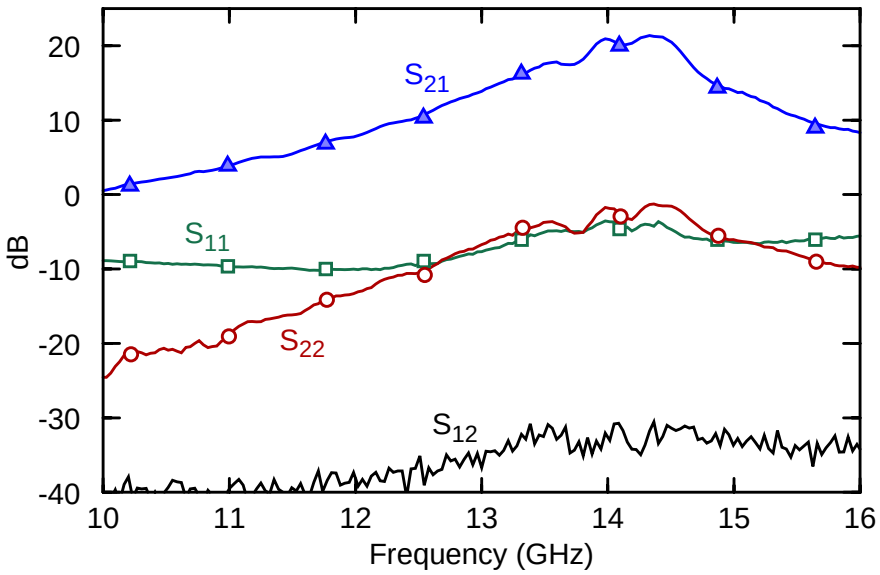


Figure 3-17 Measured S-parameters for differential LNA with source-follower buffers.

decreasing channel length due to increased hot-carrier-induced noise) and the body resistance can greatly influence the noise figure. According to SPICE simulations, increasing γ to 2, and R_{sub} from 10 to 20 Ω, increases the noise figure by 2 dB. Finally, BSIM3v3's modeling of the transistor's noise parameters is not very accurate; therefore, BSIM3v3's optimal noise matching condition versus the actual optimum can be very different. This can result in operating at a suboptimal input noise-matching condition. All of these effects taken together can yield the 4.7-dB increase in noise figure.

Figure 3-17 shows the measured S-parameters for the differential LNA with source-follower buffers (driving a 100-Ω load). For V_{gc}=0.5 V, the gain of the LNA/buffer circuit increases to 21 dB, while consuming a total of 28.2 mW from a 1.5-V supply. Table 3-5 summarizes the measured results. The resonant frequency has increased to 14.4 GHz. The gain is increased compared to the single-stage LNA result due to removal of the capacitive transformer and the presence of negative conductance at the output nodes of the LNA. Too much negative conductance, however, can result in unstable operation by

causing the total resistance at the output node of the LNA to be negative. By increasing V_{gc} to 0.9 V, the gain of the LNA/buffer circuit could be increased to 25 dB; however, S_{22} becomes greater than 1, indicating unstable operation. Therefore, V_{gc} is chosen such that stability is ensured (i.e., $S_{22} < 0$ dB).

3.6 A 23.8-GHz, 0.1-µm SOI CMOS Tuned Amplifier

3.6.1 Circuit Implementation

Since the wireless clock distribution system requires RF circuits operating above 15 GHz, it is necessary to evaluate the potential of deep submicron CMOS technologies for this frequency range. As CMOS technologies approach the sub-tenth-micron regime, the cutoff frequencies will exceed 100 GHz. Also, multiple interconnect layers in these processes will facilitate on-chip passive components with acceptable quality factors. These trends point to CMOS being a viable option for RF applications at 18 GHz and above. Recent results which attest to this fact include a 0.18-µm distributed amplifier used as a 16.6-GHz oscillator [Kle99], a 0.18-µm, 23-GHz amplifier using a simple cascode and on-chip transmission lines for matching [Yan99b], and a 0.1-µm, 25.9-GHz voltage-controlled oscillator [Hun00b]. From these, it can be seen that CMOS transistors can be used to implement circuits operating above 20 GHz.

To further investigate the RF potential of deep submicron CMOS technology including noise and linearity performance, and to evaluate the utility of lumped passive components in 20-GHz amplifiers, a tuned amplifier operating at 23.8 GHz has been implemented [Flo01b] in a partially-scaled 0.1-µm silicon-on-insulator (SOI) CMOS technology from IBM. The process uses a 0.35-µm design rule set for all dimensions except for the 0.1-µm effective gate length (0.15-µm drawn gate length) and 3-nm gate

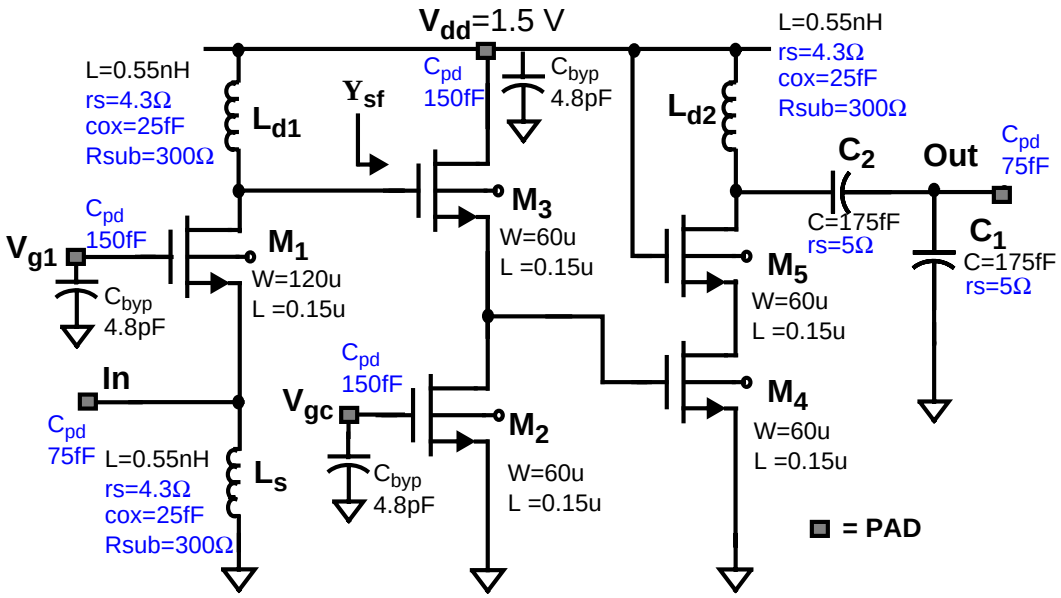


Figure 3-18 Schematic of 23.8-GHz amplifier in a 0.1-µm SOI CMOS technology.

oxide thickness. Two metal layers (0.7 µm each) are supported and the substrate resistivity is 1-2 Ω-cm. Partially-depleted, floating-body SOI transistors are used for all circuitry.

Figure 3-18 shows a schematic of the fully-integrated tuned amplifier including, important parasitics. A three-stage topology is used to boost the circuit gain and reverse isolation. As can be seen, this topology is very different than the single-stage source-degenerated LNAs previously presented, providing a look at the high-frequency performance of other circuit topologies. For ease of input matching, a common-gate input stage with a shunt inductor is used. An overview of the common-gate topology is contained in section 2.2 and Appendix A. At resonance, the input impedance to the amplifier is $1/g_{m1}$. Therefore, g_{m1} is designed to be 0.02 Ω^{-1} to provide a 50-Ω match. Following the input stage is a source-follower buffer which then drives a common-source cascode stage with a tuned load. The output of this stage is matched to 50 Ω using a capacitive transformer. This stage is a non-degenerated version of the LNAs discussed earlier. Figure

3-13(b) shows a die photograph of the 0.1-μm LNA. The die size is 0.44x0.51 mm^2. Ground-shielded diamond-shaped pads are used at the input and output to reduce the parasitic capacitance to the substrate. Three on-chip spiral inductors of 0.55 nH are used in the circuit. Finally, on-chip accumulation-mode MOS capacitors of 4.8 pF are used to bypass V_{dd}, V_{g1}, and V_{gc}.

3.6.2 Source-Follower

The source-follower is used to shift the dc bias level from the output of the first stage (at V_{dd}) to the input of the third stage. The bias point of the source-follower is controlled through input V_{gc}, which controls the current through M_2 and sets the V_{gs} of M_3. A source-follower with a capacitive load can have a negative input conductance. Since inductive source-degeneration provides a positive, real input impedance for the transistor, by reason it follows that capacitive source-degeneration provides a negative, real input impedance for the transistor.

Referring to Figure 3-18, it can be shown that the input admittance looking into M_3 is as follows:

$$Re(Y_{sf}) = G_{sf} = \frac{\omega^2[g_T C_{gs3}^2 - g_{m3} C_{gs3} C_{LT}]}{(g_{m3} + g_T)^2 + \omega^2 (C_{gs3} + C_{LT})^2}, \quad (3.2)$$

$$Im(Y_{sf}) = B_{sf} = \frac{\omega C_{gs3}(g_{m3} g_T + g_T^2 + \omega^2 (C_{gs3} C_{LT} + C_{LT}^2))}{(g_{m3} + g_T)^2 + \omega^2 (C_{gs3} + C_{LT})^2} + \omega C_{gd3}, \quad (3.3)$$

where g_T is the total output conductance at the source-follower output node (equal to $g_{ds3}+g_{ds2}$) and C_{LT} is the total capacitance at the same node (equal to $C_{gs4}+C_{sb3}+C_{db2}+C_{gd2}$). The voltage gain through the source-follower buffer is as follows:

$$A_{v,\,sf} = \frac{g_{m3} + j\omega C_{gs3}}{g_{m3} + g_T + j\omega (C_{gs3} + C_{LT})}, \quad (3.4)$$

which has a magnitude less than one, a pole at $\omega=(g_{m3}+g_T)/(C_{gs3}+C_{LT}) < \omega_T$, and a zero at $\omega\cong\omega_T$. Negative conductance indicates that energy is being generated. When a source-follower is used after an amplifier containing an inductive load, this energy actually replenishes some of the energy lost in the inductor, causing the quality factor to increase. Hence, the negative conductance of the source-follower increases the gain of the LNA through increasing the load quality factor.

Figure 3-19 shows the measured input conductance versus control voltage (V_{gc}), versus frequency for a source-follower implemented in the 0.25-μm CMOS test chip. This buffer is driving an open pad structure having a capacitance of ~ 40 fF. The conductance becomes more negative with increasing frequency in agreement with (3.2). Also, the conductance becomes more negative as V_{gc} increases to 1.2-1.4 V, and then begins to become less negative for further increases in V_{gc}. This is due to g_{m3} increasing for V_{gc} between 0 to 1.2 V, causing G_{sf} to decrease. However, the transistors in the source-follower eventually enter the linear regime, causing g_T to increase and g_{m3} to decrease; thus, G_{sf} becomes less negative.

3.6.3 Gain of 24-GHz LNA

The voltage gain of the three-stage LNA can be readily derived using equations (A.3), (3.4), and (2.23). Assuming $G_{sf} < 0$, the total voltage gain is as follows:

$$\left|A_v\right|_{\omega=\omega_o} = \left|A_{v,\,cg}\cdot A_{v,\,sf}\cdot A_{v,\,cs}\right| \tag{3.5}$$

$$= \left(\frac{g_{m1}Q_{Ld1}^{eff}\omega_o L_{d1}}{1+g_{m1}R_S}\right)\left|A_{v,\,sf}\right|\left(\frac{1}{2}g_{m4}Q_{Ld2}\omega_o L_{d2}\left|\frac{\delta(\omega_o)}{n(\omega_o)}\right|\right)$$

$$= \left(\frac{g_{m1}Q_{Ld1}^{eff}\omega_o L_{d1}}{1+g_{m1}R_S}\right)\left|\frac{g_{m3}+j\omega C_{gs3}}{g_{m3}+g_T+j\omega(C_{gs3}+C_{LT})}\right|\left(\frac{1}{2}g_{m4}Q_{Ld2}\omega_o L_{d2}\left|\frac{\delta(\omega_o)}{n(\omega_o)}\right|\right)$$

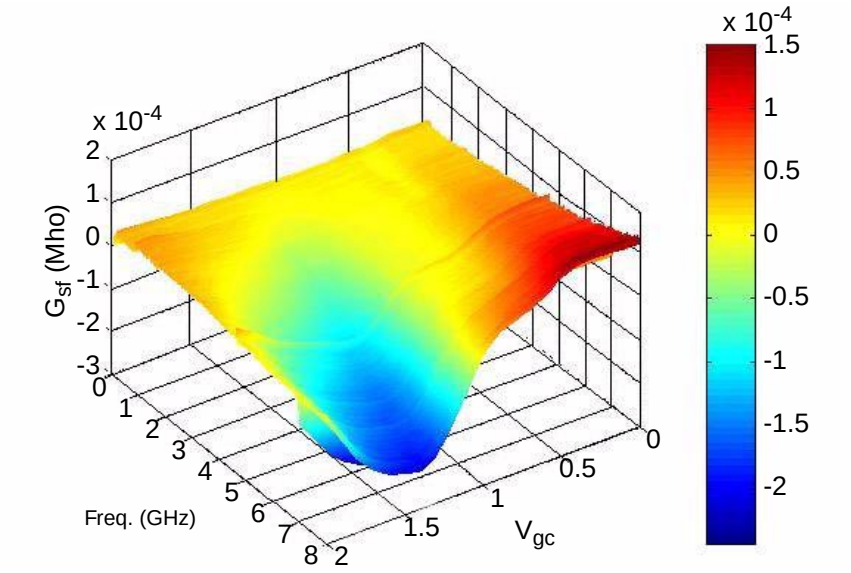


Figure 3-19 Input conductance to source-follower buffer driving a capacitive load versus frequency and control voltage.

where the factors δ and *n* have been defined in (2.24) and (2.25), and $A_{v,sf}$ is defined in (3.4). An effective quality factor has been introduced for L_{d1}, to account for the negative input conductance of the source-follower buffer, as follows:

$$Q_{Ld}^{eff} = \frac{Q_{Ld}}{1-(|G_{sf}| \cdot Z_{Ld}(\omega_o))}. \tag{3.6}$$

Impedance Z_{Ld} is the conductance of the drain inductor of the first stage at (tank) resonance. Such a substitution for the quality factor can be used whenever a tuned gain stage is followed by a source-follower buffer. With the input impedance designed to be R_S=50 Ω (i.e., g_{m1} = 0.02 Ω^{-1}) and with L_{d1}=L_{d2}, the total forward transducer gain becomes

$$|S_{21}| = 2 \cdot |A_v|_{\omega = \omega_o} = \frac{1}{2}\frac{g_{m4}}{R_S} Q_{Ld1}^{eff} Q_{Ld2} \omega_o^2 L_{d1}^2 \cdot |A_{v,\,sf}| \left|\frac{\delta(\omega_o)}{n(\omega_o)}\right|. \tag{3.7}$$

It can be seen that the denominator of (3.6) can become zero, indicating that “infinite” gain is obtained. Thus, a finite output signal can be obtained when no input is present to the amplifier, meaning that the circuit will oscillate. Obviously, this condition is to be

avoided. Thus, the conductance of the source-follower is adjusted such that the gain is improved while stability is maintained.

3.6.4 Measured Results

The measured S-parameters of the SOI amplifier are shown in Figure 3-20(a). At 23.8 GHz the amplifier is perfectly matched to 50 Ω at the input, with an S_{11} of -45 dB, and well-matched at the output, with an S_{22} of -9.4 dB. The transducer gain (S_{21}) is 7.3 dB while the reverse isolation is 27 dB, which are both excellent for a CMOS circuit at this frequency range. Also, the gain is greater than 0 dB beyond 26 GHz. The total supply current is 53 mA for a 1.5-V supply, which is high due to the use of multiple amplifier stages.

The measured quality factor (Q) of the on-chip spiral inductors is ~2 at 24 GHz. This value is lower than the expected value of 4.8, which resulted in the gain being ~15 dB ($20\log\{4.8/2\}^2$) lower than its simulated value of 22 dB. The reason for this Q degradation, however, is not fully understood.

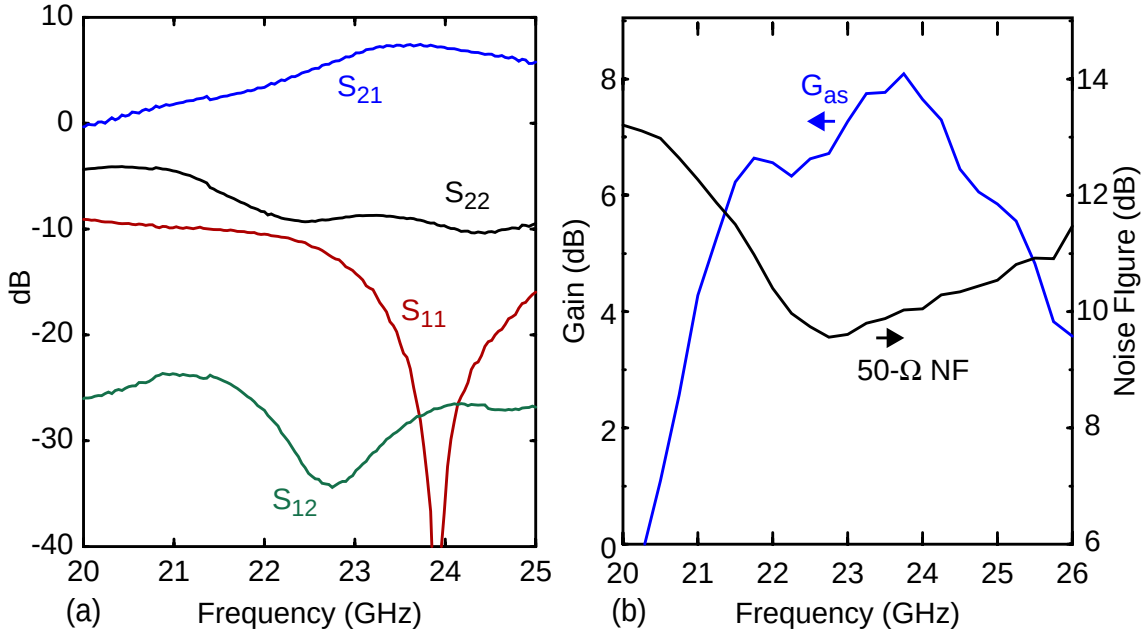


Figure 3-20 (a) Measured S-parameters and (b) measured operating power gain (G_P) and 50-Ω noise figure (NF) vs. frequency.

Examining these results, it can be concluded that the gain performance of this 23.8-GHz amplifier is limited primarily by the inductor quality factor. Since this design was completed before the effects of substrate resistance on inductor Q [Flo00b] were fully understood, patterned ground shields were not used even though the substrate resistivity of 1-2 Ω-cm is in the range where ground shields would have enhanced the inductor Q. The substrate resistance for these inductors is on the order of 300 Ω, while the parasitic capacitance to the substrate is 25 fF (refer to inductor model in Figure 3-1(a)). According to equation (3.1), the inductor Q is greatly reduced at 24 GHz, due to the substrate resistance. In fact, had patterned ground shields been used, then the substrate resistance would have been reduced to ~10-15 Ω, while the parasitic capacitance would have increased. This would have approximately doubled the inductor Q, potentially increasing the gain by $20\log\{2\}^2$=12 dB (for the case when the source-follower is adjusted for close to zero input conductance). Further improvements could be obtained by improving the back-end process by increasing the top-level metal thickness, increasing the distance between the top-level metal and the substrate, and using copper rather than aluminum for the metal (as will be the case for fully-scaled 0.1-μm technology). Such improvements should easily lead to inductor Q > 30 [Bur98] at 20 GHz, as has been shown in this chapter. This would dramatically increase the amplifier gain and decrease the power consumption.

Using simulated values for all quantities except Q_{Ld} in (3.7), and then inserting the extracted Q_{Ld} value of 2, results in S_{21} = 9.2 dB, which is close to the measured S_{21}. The discrepancy is attributed to differences between the transistor model and the actual device. The estimated input conductance to the source-follower is -2 mS, resulting in a Q^{eff} of 2.8. Therefore, the negative conductance of the source-follower improves S_{21} by a factor of

~1.4 or 3 dB. However, $|A_{v,sf}|$ is ~0.7; therefore, the net gain in S_{21} due to the source-follower is 1.4*0.7 ≅ 1 (0 dB). Thus, for this amplifier, while the source-follower is providing a needed dc level shift between stages 1 and 3, the gain is unaffected. A potential better use for the source-follower would be to use it purely as a negative conductance generator, without passing a signal through the stage. The power consumption could be reduced by reusing the current in the gain stage with the source-follower.

Multistage amplifiers can exhibit poor linearity, and negative conductance can potentially affect this linearity even further. The measured P_{1dB} is -10 dBm (-16.2 dBm referred to the input), while the IIP3 is -7.8 dBm. These linearity data are considerably better than those obtained in [Ho98], an encouraging result, indicating that acceptable linearity can be achieved with amplifiers utilizing source-followers.

Figure 3-20(b) shows the measured noise figure (NF) and associated gain (G_{as}) versus frequency. The gain is 8.1 dB at 23.8 GHz, while the noise figure is very high at 10 dB. The high noise figure is caused by the reduced first-stage gain, due to the low inductor Q. Also, the noise associated with the input inductor, L_S, increases NF as well. The low gain allows noise from stages two and three to refer to the input of the circuit. While such a noise figure certainly is too high for typical wireless communication systems, it can be decreased through circuit and inductor optimization. A final clarification on the amplifier's performance is that although the NF is larger than the gain, it does not mean that the amplifier is unusable (i.e., that the output signal-to-noise ratio (SNR) will always be < 1). Noise figure is a relative quantity, representing *degradation* of SNR. Therefore, a high NF degrades the dynamic range of a circuit through raising the minimum detectable signal.

Table 3-6 Summary of measured results for 23.8-GHz SOI CMOS tuned amplifier.

Parameter	Result	Parameter	Result
Resonant Frequency	23. 8 GHz	NF	10 dB
S_{21}	7.3 dB	P_{1dB}(in)	-16.2 dBm
S_{11}	-45 dB	IIP3	-7.8 dBm
S_{22}	-9.4 dB	V_{dd}	1.5 V
S_{12}	-27 dB	Supply Current	53 mA

A summary of the results for the tuned amplifier is shown in Table 3-6. Excellent gain and isolation is obtained for CMOS circuits at this frequency. While only moderate noise and linearity performance are obtained, once a fully-scaled CMOS technology with a more advanced back-end process is used, the results should dramatically improve. These improvements will be due to increased inductor Q, decreased parasitic capacitance which allows the inductance and hence gain to increase, and finally further circuit optimization. Finally, these results show that a 0.1-μm CMOS technology should be to able support RF applications above 20 GHz, and suggest even higher operating frequencies for further scaled CMOS technologies.

3.7 Summary

The validity of the LNA design methodologies presented in the previous chapter was demonstrated through implementation of a 0.8-μm, 900-MHz CMOS LNA achieving a 1.08-dB minimum noise figure at 30 mW, and a 1.5-dB minimum noise figure at 8 mW. These results meet all of the required performance metrics for LNAs, demonstrating the competitiveness of CMOS LNAs as compared to GaAs or silicon bipolar technologies. Using a 0.25-μm CMOS process, 8-GHz single-ended and differential LNAs have been

implemented on both p^+ and p^- substrates. The differential LNA on p^- substrate provides 10-dB of gain, with a 4.9-dB noise figure, consuming 21 mW from a 2.5-V supply. Using a p^+ substrate degrades the gain by ~ 6 dB and the noise figure by ~ 2.5 dB, due primarily to reduced inductor Q.

A 13.3-GHz differential source-degenerated LNA with 8 dB of gain has been implemented in a 0.18-μm CMOS technology. The circuit was designed to operate at 21 GHz; however, larger than expected inductance and transistor capacitance decreased the resonant frequency. This shows that as the operating frequency of the circuit increases above 10 GHz, modeling of the transistors and passive components becomes increasingly important. Currently, the accuracy is not scaling with frequency, indicating that larger deviations between simulated and measured performances will occur at higher frequencies. Although copper interconnects have increased the inductor Q in the 0.18-μm technology, an unplanned thinning of the metal layer during fabrication has mitigated the overall improvement. Even still, inductor Q's of ~28 at 15 GHz have been obtained. A test-circuit containing the differential source-degenerated LNA plus a pair of source-followers has been implemented, showing a gain of 21 dB at 14.4 GHz.

Finally, using a 0.1-μm partially-scaled SOI CMOS technology, a multistage tuned amplifier with a common-gate input and source-followers has been implemented. Source-followers generate negative conductance and provide a dc level-shift. The input admittance and gain of this stage were presented. This amplifier achieves 7.3 dB of gain at 23.8 GHz, with positive gains beyond 26 GHz. This result is comparable to the highest operating frequency to date [Yan99b] for CMOS amplifiers.

CHAPTER 4
CMOS FREQUENCY DIVIDERS

4.1 Overview

In the clock receiver, the frequency divider translates the global clock signal to the local clock signal. The divider should have a maximum operating frequency above 15 GHz and should dissipate a minimal amount of power. In addition, the divider should be capable of locking to very low-level input signals--specified in terms of input sensitivity--which will improve the minimum detectable signal (MDS) of the clock receiver. Finally, the signals reaching each of the frequency dividers within the clock receivers will potentially have different phases and amplitudes, both resulting in clock skew, as well as random noise, resulting in clock jitter. Clock skew and clock jitter as a result of these mechanisms will be discussed in Chapter 5. However, to account for the phase difference and, hence, reduce the clock skew, the dividers should be synchronized between receivers.

Using silicon and SiGe bipolar technologies, frequency dividers operating up to 82 GHz have been reported [Was00a, Was00b, Kna00, Wur00], and using CMOS technologies, dividers operating up to 26.5 GHz have been reported [Wan00, Wet00, Raz94, Kur97]. Clearly, silicon is capable of supporting divider circuits operating above 20 GHz. In this chapter, the design and implementation of high-frequency CMOS frequency dividers operating up to 18.75 GHz and employing either source-coupled logic (SCL) or dual-phase dynamic pseudo-NMOS $[DP]^2$ logic [Biy96, Yan99a] will be presented. The SCL dividers are implemented in 0.25- and 0.18-μm bulk CMOS technologies, operating

up to 10 and 15.8 GHz, respectively. The $[DP]^2$ divider is implemented in a partially-scaled, 0.1-μm CMOS technology with bulk and SOI substrates. A design methodology for SCL dividers based on injection locking which allows for maximizing the operating frequency and minimizing the required voltage swing of the divider's input signal is discussed. Also, using SCL, a new programmable divider is developed which allows the start-up state of the divider to be controlled. Such programming will decrease the systematic clock skew, provided that the dividers are properly initialized and synchronously released from the start-up state. The initialization and start-up methodology for the dividers are also presented in this chapter.

4.2 Frequency Divider Using Source-Coupled Logic

4.2.1 Circuit Description

Figure 4-1(a) shows a block diagram of a divide-by-eight (8:1) frequency divider employing SCL. The divider consists of three cascaded 2:1 dividers with dual-phase inputs and outputs. Each 2:1 divider, shown in Figures 4-1 (b) and (c), consists of two SCL D-latches in a master-slave configuration [War89, Flo00a, Hun01]. The outputs are tied to the inputs with inverted phase to perform a toggle operation.

Source-coupled logic (also known as MOS current-mode logic (MCML)) has some distinct advantages for the wireless interconnect application. First, a small-level input voltage can be detected on the clock input. This is due to the differential structure of the latch as well as the mechanism of division, which will be discussed shortly. Therefore, the input sensitivity for the divider is high, improving the MDS of the receiver. Second, the latch can be designed such that the outputs do not swing rail-to-rail, decreasing the

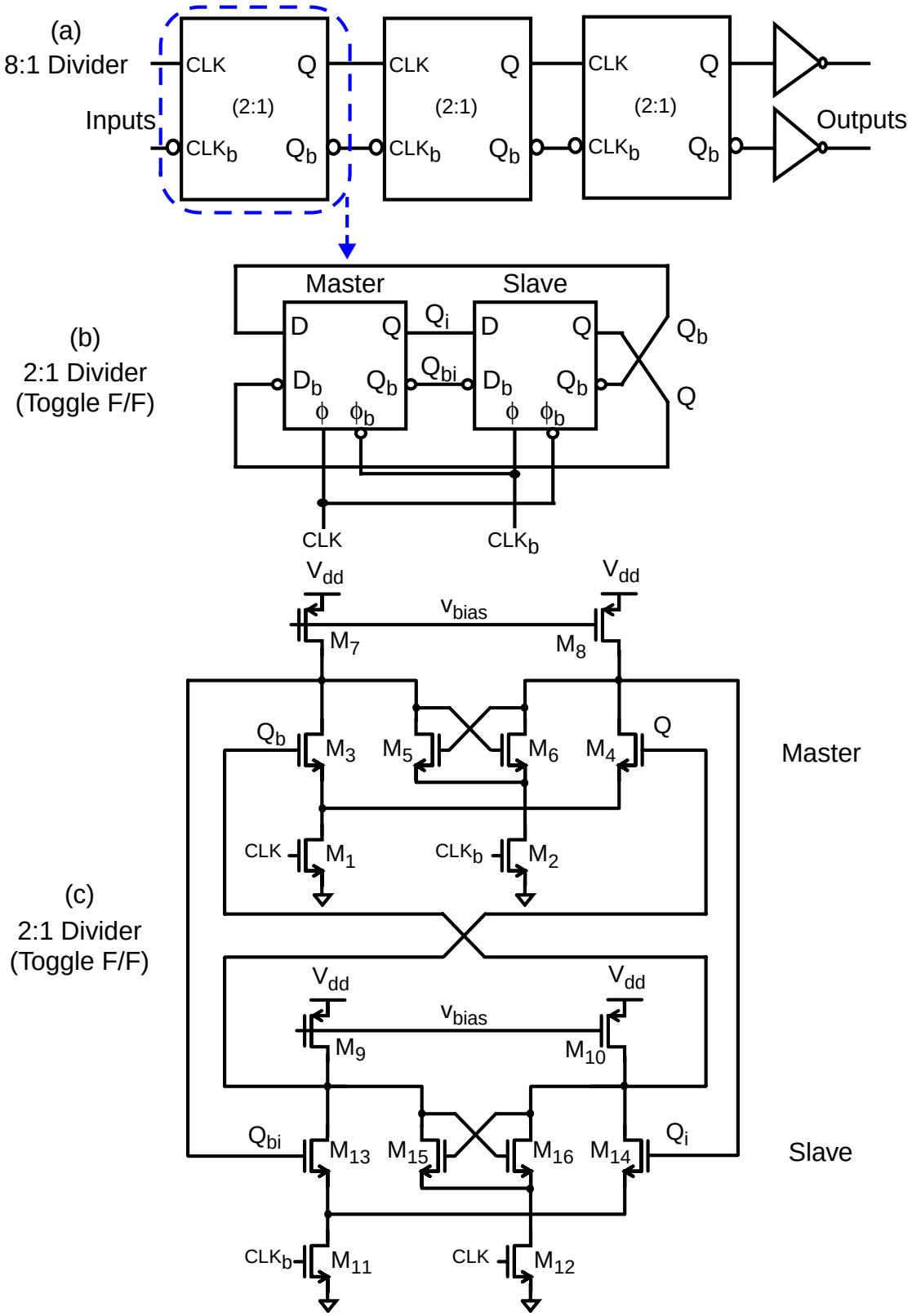


Figure 4-1 Block diagrams of (a) 8:1 divider consisting of three cascaded 2:1 dividers, and (b) 2:1 divider consisting of two D-latches in master/slave. (c) Schematic of 2:1 divider implemented using source-coupled logic.

power consumption for a given operating frequency. Third, the use of a differential structure reduces the switching noise of the latch, by keeping the supply current approximately constant. Thus, the noise added by the divider is reduced, improving the output jitter.

A conventional SCL latch has a current source between the sources of $M_{1,2}$ and $M_{11,12}$ and ground, resulting in constant tail current. This current source is omitted for low voltage operation due to the limited supply head-room, causing the total current flowing through the evaluate and hold stages to not be constant. However, for fast transitions, the 2:1 divider always has both an evaluate and a hold stage on, thus the supply current remains relatively constant (reducing the switching noise).

The voltage V_{bias} is grounded to increase the maximum operating frequency by operating $M_{7,8}$ in the linear region, which lowers the RC time constant for nodes Q and Q_b. Furthermore, when the voltage of Q is increasing (during a low to high transition), the drain-to-source voltage and the output resistance of M_9 (in linear region) are decreasing. This nonlinearity of M_9 helps to pull up Q to its logic high, which in turn helps to increase the maximum operating frequency at the same power consumption. Similarly, when Q is decreasing, the nonlinearity tends to push down Q to its logic low. In addition to the advantage of high speed operation, this topology has reduced power consumption compared to the topology in [Cra95], due to the elimination of the folded diode-connected transistors from Q and Q_b to ground.

4.2.2 Latched Operating Mode

The 2:1 divider implemented with SCL can operate in one of two modes. The first mode is the standard digital operation of latching, while the second is an injection-locked mode which will be presented in the next section. The latching mode of operation occurs

when the input clock signals have a large voltage swing. Here, $M_{3,4}$ act as an evaluation stage when the latch is transparent, and regenerative pair $M_{5,6}$ act as a hold stage when the latch is opaque. Thus, for CLK = high, the master is transparent and the slave is opaque, with Q_i and Q_{bi} taking the value of D and D_b. For CLK = low, the master is opaque and the slave is transparent, and nodes Q_i and Q_{bi} are passed to the output. As is evident from this description, cascading two level-sensitive D-latches in a master-slave configuration results in an edge-triggered D-flip-flop (DFF). It can easily be verified that connecting the outputs of a DFF back to its inputs with inverted phase results in a toggle flip-flop. Thus, for every clock pulse, the output is toggled, resulting in a divide-by-two operation.

4.2.3 Quasi-Dynamic Operation

The question arises as to whether or not this SCL latch is static or dynamic. In other words, is there a lower frequency limit for this latch? The answer to this question depends on the sizing of the transistors in the latch [Mur95], and because of this, the latch topology is *quasi-dynamic*. To illustrate this, the PMOS load transistors are first modeled as resistors, with a resistor R_{PM}. Consider the case when the output of the master D-latch, Q_{bi} is first evaluated low and then held low. Since there is no tail-current source, the currents through M_1 and M_2 are not necessarily equal. The current values depend on the sizing of M_1 and M_2 and the input clock signals. The current pulling Q_{bi} low during evaluation for the master DFF is then modeled as $f_1(I_1)$, where f_1 depends on the sizing of M_3 and M_4, the voltages Q and Q_b, and the evaluation current, I_1. Thus, Q_{bi} has a voltage during evaluation equal to

$$LOW_{Eval} = V_{dd} - f_1(I_1)R_{PM7}. \tag{4.1}$$

Likewise, during hold operation of the master D-latch, the current pulling Q_{bi} low is modeled as $f_2(I_2)$, where f_2 depends on the sizing of M_5 and M_6, the voltages Q_i and Q_{bi}, and the hold current, I_2. Thus, Q_{bi} has a voltage during hold equal to

$$LOW_{Hold} = V_{dd} - f_2(I_2)R_{PM7}. \tag{4.2}$$

If $f_2(I_2) > f_1(I_1)$, the output voltage swing of the latch is decreased, and the voltages Q_i and Q_{bi} might not be large enough to drive the next master-slave flip-flop.

For a given $f_1(I_1)$ to $f_2(I_2)$ ratio, a lower frequency limit for the 2:1 divider exists, set by how fast the nodes can change from LOW_{Eval} to LOW_{Hold}. As long as the input frequency is high enough, then LOW_{Eval} cannot fully charge to LOW_{Hold}, and the divider functions properly. This lower-frequency limit was observed in simulations, where the minimum frequency was approximately one-eighth of the maximum frequency for the chosen transistor widths. To make the quasi-dynamic latch fully static, first, tail current sources should be added and W_1 should be set equal to W_2. This then makes I_1 equal to I_2. Second, the widths of $M_{3\text{-}6}$ should all be equal [Mur95], forcing $f_1(I_1)$ to be equal to $f_2(I_2)$.

4.3 Injection Locking of SCL Frequency Divider

The second mode of operation for the 2:1 SCL divider is injection locking. Injection locking is the process of synchronizing an oscillator with an incident signal. Oscillators can be injection-locked to the fundamental [Adl46, Pac65, Uzu85], subharmonics [Zha92], and superharmonics [Sch71, Rat99] of the input signal. This section will examine the oscillation of the SCL divider and discuss how the divider can be injection-locked. The actual theory behind injection locking is presented in Appendix E. This appendix reviews the basic operation of injection-locked oscillators (ILO's), and presents the

locking range, its dependence on signal level, the steady-state phase error between input and output signals, and the phase noise of ILO's.

4.3.1 Oscillation of SCL Divider

To understand the phenomenon of injection locking, the oscillation of the 2:1 divider with no input present must first be understood. When the input clock signal swings are very small, then CLK and CLK_b are approximately equal at their common-mode value. Thus, both the master and slave latches are semi-transparent, allowing signals to propagate through both latches. Referring to Figure 4-1(b), if the delay from the gate to the drain of M_3 is equal to τ_{pd}, then the total delay around the loop is equal to $4\tau_{pd}$. Thus, the divider oscillates at a frequency equal to $\frac{1}{4\tau_{pd}}$ and the signal at the drain of M_3 will lag the signal at the gate of M_3 by 90^o. The divider circuit can thus be likened to a two-stage ring oscillator with an inversion in the loop[1].

Additional understanding of the oscillator can be gained by solving for the small-signal loop gain of the divider. First, assume the two latches are identical and that each latch is symmetric (i.e., W_3=W_4, W_5=W_6, and W_7=W_8). Consider the case when CLK and CLK_b are held at a constant and equal value. For this case, M_1 and M_2 become current sources. Cross-coupled transistors $M_{5,6}$ can be represented as negative resistances with values of $-1/g_{cc}$, where g_{cc} is the transconductance of M_5. The PMOS load can be modeled as a conductance, g_P. Finally, the total capacitance at the output nodes of the latch can be represented by C_L. Figure 4-1(c) can then be simplified to Figure 4-2, by

1. An actual expression for the propagation delay through each latch was not derived, since this delay can readily and more accurately be obtained with SPICE.

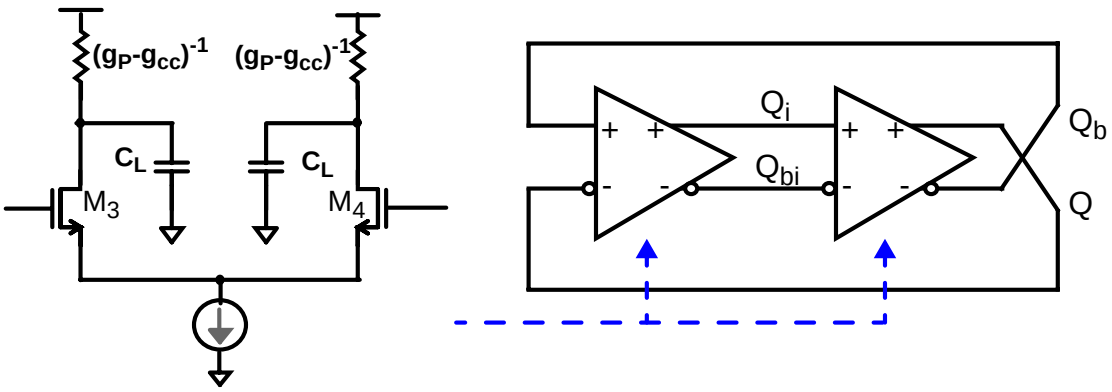


Figure 4-2 Representation of source-coupled latch as a fully-differential amplifier and the 2:1 divider as an oscillator.

representing each source-coupled latch as a fully-differential amplifier. The small-signal loop gain (T) of the 2:1 divider can be shown to be as follows:

$$T = -\left(\frac{g_{m3}}{g_P - g_{cc} + j\omega C_L}\right)^2. \tag{4.3}$$

For oscillations to begin, the phase of T should be 360^o and $|T| > 1$. Choosing $|T| > 1$ ensures start-up and causes the amplitude of oscillation to increase until non-linearities within the amplifier limit the amplitude. This amplitude condition requires $g_{m3} > \omega_o C_L$. For the phase of T to be 360^o, the phase-shift through each differential amplifier should be 90^o. This corresponds to $g_P = g_{cc}$. This Barkhausen criterion for oscillators applies to small-signal sinusoidal oscillations. However, with a loop gain greater than one, the oscillator will become nonlinear and its amplitude and frequency will be determined by the large-signal characteristics of the circuit. The divider then behaves as a relaxation oscillator (also known as an astable multivibrator) [Sed91].

Relaxation oscillators are hysteretic comparators which charge and discharge capacitances located in a feedback loop. The oscillation frequency of a relaxation oscillator depends on the capacitance being charged, as well as the current drive of the

comparator. It is interesting to note that any ring oscillator whose propagation delay is set by the charging of RC circuits can be considered to be a relaxation oscillator [Ega99]; thus, the two models used to describe the divider's oscillation are equivalent.

4.3.2 Description of Injection Locking

Since the 2:1 divider can self-oscillate, it is possible to injection-lock the divider to an input signal whose frequency is close to either the fundamental, subharmonic, or superharmonic of the oscillation frequency. Thus, for a 2:1 injection-locked frequency divider (ILFD), the input signal is close to the second harmonic of the oscillation frequency, herein referred to as f_{iSO}. The locking mechanism of the oscillator, for an input signal at twice the natural frequency (a superharmonic), is created by nonlinear properties in the oscillator which generate intermodulation products close to the natural frequency [Rat99]. Referring to Figure 4-1(c), the drain node of M_1 oscillates at twice the natural frequency; hence, this node is naturally suited to injecting a signal at this double frequency. An alternative and equivalent understanding of the circuit is that injection locking is being used to synchronize this "double-frequency" oscillator (drain of M_1) at a frequency near f_{iSO}. This understanding is more straightforward and avoids the complications surrounding superharmonic injection locking.

The range of input frequencies over which the ILFD can be locked or "pulled" is a function of the input voltage swing and the frequency-dependent energy-loss in the oscillator. Appendix E shows that the voltage swing of the locking signal (V_L) is related to the locking frequency range ($\Delta\omega_o$) and the oscillator output voltage swing (V_O), as follows:

$$\frac{V_L}{V_O} > \Delta\omega_o A. \tag{4.4}$$

Here, V_O is the voltage swing of the double-frequency oscillator (drain of M_1), and A is equal to the derivative of phase-shift around the oscillator with respect to frequency. For a tuned oscillator, A is equal to $2Q/\omega_o$. Appendix F shows that the equivalent quality factor of a ring-oscillator is approximately equal to $\pi/2$. Thus, an injection-locked ring oscillator has the following input-swing to locking-range relationship (also known as the input sensitivity of the divider):

$$\frac{V_L}{V_O} > \left(\frac{\Delta\omega_o}{\omega_o}\right) \cdot \pi . \tag{4.5}$$

A voltage conversion gain can be defined for the frequency divider, equal to the ratio of the output swing to the input swing. Since the gain occurs at two different frequencies, it is referred to as conversion gain. This gain can be related to (4.5) by relating the output swing of the divider to the swing of the double-frequency oscillator. Thus, the circuit has "infinite" gain at f_{iSO}. Also, (4.5) shows that the further away the input frequency is from f_{iSO}, the larger the input voltage-swing has to be.

To control the oscillation frequency and conversion gain of the divider, the transistor sizes, input common-mode voltage, and supply voltage can all be adjusted. Referring to Figure 4-1(c), the speed of switching node $Q_{i,bi}$ HIGH depends on the size and $|V_{gs}|$ of $M_{7,8}$ (note V_{dd} dependence), while the speed of switching node $Q_{i,bi}$ LOW depends on the sizes of $M_{3,4}$ and $M_{1,2}$ as well as the common-mode voltage on the clock inputs. For both cases, the switching speed is decreased by the presence of regenerative pair $M_{5,6}$, since the positive feedback has to be overcome by the charging or discharging mechanism. Therefore, all of the transistor sizes, the supply voltage, and the clock common-mode voltage determine the self-oscillation frequency for the 2:1 ILFD. Note that the transistor sizes are

used to adjust the oscillation frequency during design, while the voltages can be used to adjust the oscillation frequency during circuit testing.

4.3.3 Simulation of Injection-Locked Divider

This section will present simulation results for an ILFD, showing the f_{iSO} and demonstrating the dependence of the input swing on the locking range. To extract f_{iSO}, the 8:1 divider is simulated using a transient analysis, with both CLK and CLK_b held at approximately mid-supply. As with other oscillator simulations, initial conditions are required, where nodes Q_i and Q are initialized to the supply and Q_{bi} and Q_b are initialized to ground. Finally, since this is an analog simulation, the SPICE tolerances should be decreased as compared to a standard digital simulation.

Figure 4-3 shows the simulated oscillation of the 8:1 ILFD, for a 0.25-µm CMOS process. Since V_{dd} = 2.5 V, CLK and CLK_b are set to ~1.3 V. The output of the first 2:1 divider is oscillating at 6.1 GHz, while the following 2:1 dividers are locked at 3.05 and

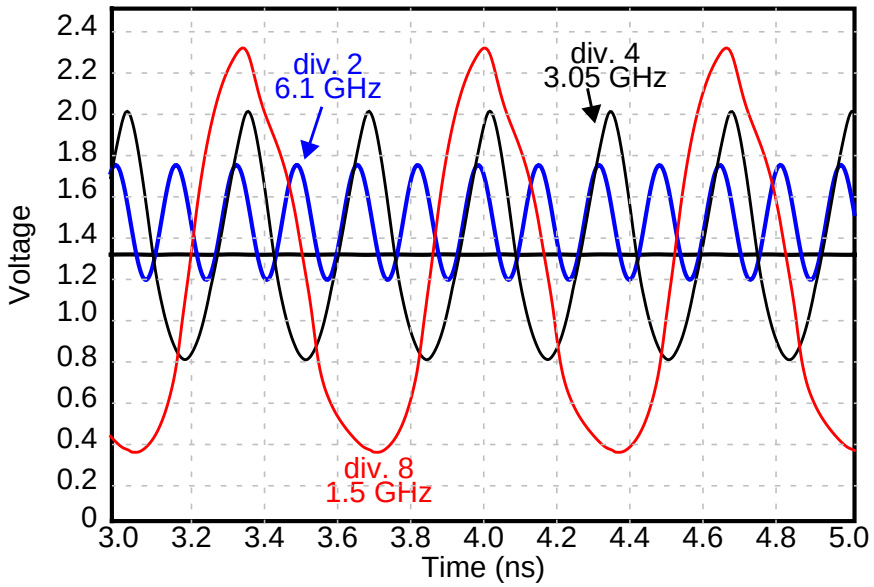


Figure 4-3 Simulation of self-oscillation of 8:1 source-coupled divider. The clock inputs are held at 1.3 V, causing the first 2:1 divider to oscillate at 6.1 GHz for V_{dd}=2.5V (f_{iSO} = 12.2 GHz).

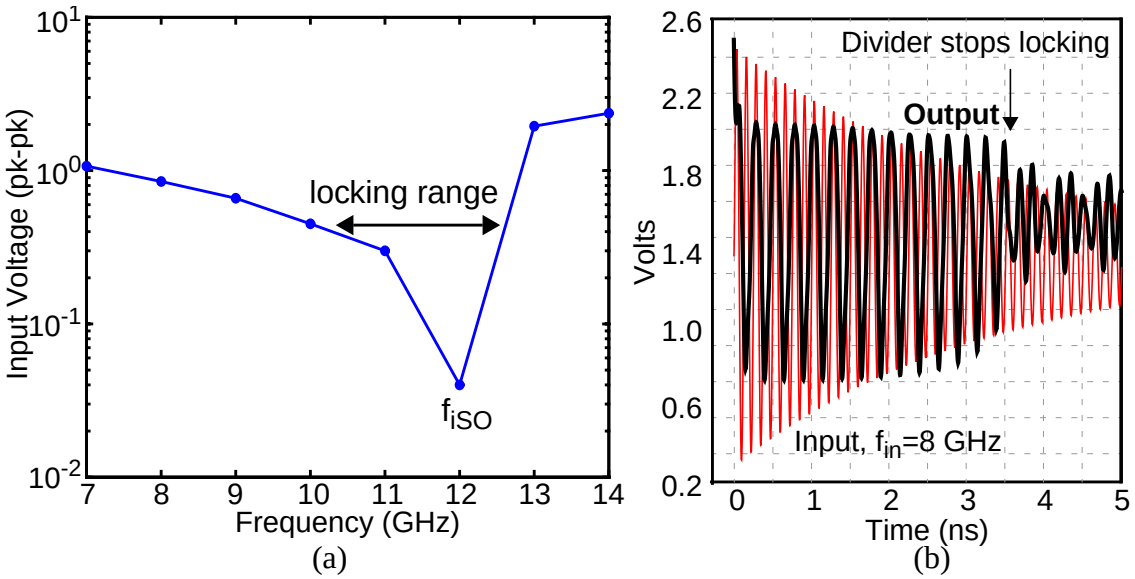


Figure 4-4 (a) Simulated input sensitivity of 0.25-µm CMOS 8:1 divider (b) Exponentially decreasing input signal at 8 GHz and output signal of 8:1 divider, illustrating divider's dependence on input voltage swing.

1.5 GHz, respectively. Thus, f_{iSO} is equal to 12.2 GHz. This simulation can be iterated through various device sizes to set f_{iSO} to the desired operating frequency. Additionally, this simulation can be run for the second and third 2:1 dividers to set their respective self-oscillation frequencies to one-fourth and one-eighth of the desired operating frequency. Note that for an 8:1 asynchronous divider, any of the three 2:1 dividers can oscillate provided that the input signal level to each divider is small. However, for the typical case where the first 2:1 divider oscillates with a large output signal, the following 2:1 dividers operate in a latched mode.

The input-swing versus locking-frequency-range relationship is shown in Figure 4-4(a), which plots the simulated input peak-to-peak voltage swing versus input frequency. To obtain these input swings using a single simulation, a damped sinusoid was injected into the divider, as shown in Figure 4-4(b). Eventually, the divider cannot lock to the input signal, at which point the input voltage swing is determined. This simulation is

repeated for every desired input frequency. As can be seen from Figure 4-4(a), the required input swing dips at the self-oscillation frequency (12.2 GHz), and then rapidly increases for higher frequencies[2]. The locking frequency range for a given input swing is equal to the distance between the left and right portions of the curve. This simulation verifies that larger input voltage swings result in larger locking ranges.

4.3.4 Implications of Injection Locking for Clock Distribution

The frequency divider will operate in the injection-locked mode for small-level input signals, and in the latched mode for large input signals. Therefore, to minimize the minimum detectable signal (MDS) of the receiver, the divider should be injection-locked, with its input-referred self-oscillation frequency near the operating frequency of the receiver. This provides an alternative interpretation for the wireless clock distribution system. Using this interpretation, each receiver is initially a free-running oscillator. The transmitted global clock signal is then used to injection-lock each oscillator and therefore synchronize the system. Noise and interference can corrupt the global reference signal as well as the phase of the oscillators themselves, resulting in phase noise or clock jitter.

4.4 A 10-GHz, 0.25-μm CMOS SCL Divider

4.4.1 Circuit implementation

A 10-GHz 128:1 source-coupled frequency divider has been implemented using a standard 0.25-μm CMOS technology. A block diagram of the divider is shown in Figure

2. Note that for wireless interconnects, the region corresponding to input frequencies above f_{iSO} should be avoided since the receiver's MDS would be severely degraded.

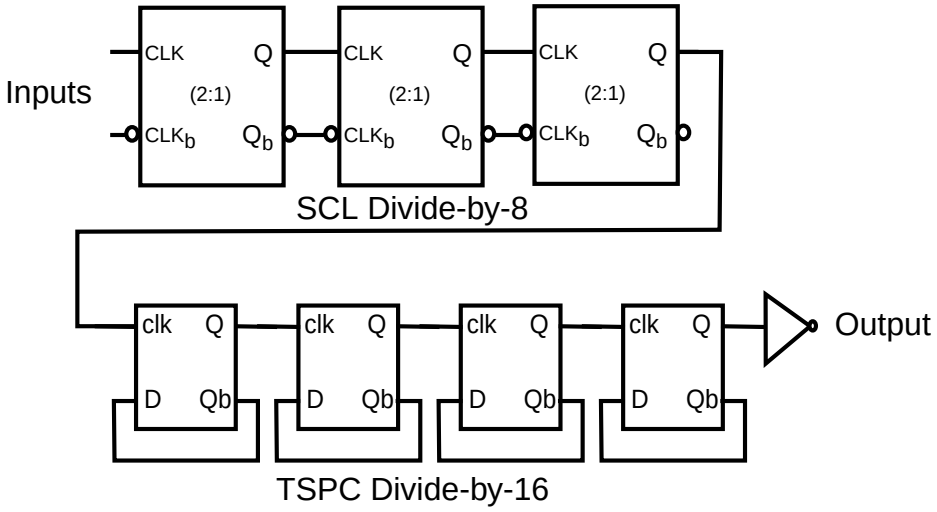


Figure 4-5 Block diagram of 128:1 divider.

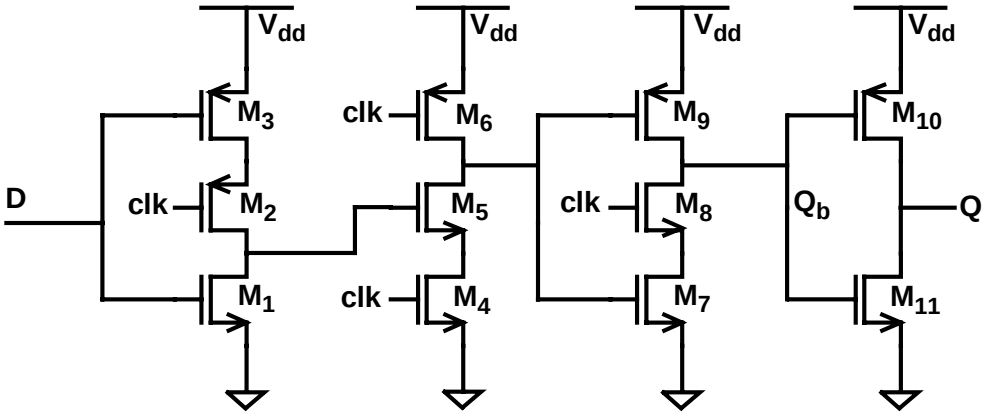


Figure 4-6 Schematic of true single-phase clocked (TSPC) latch.

4-5. The first 8:1 divider is implemented with SCL, while the lower frequency 16:1 asynchronous divider is implemented using true-single-phase-clocked (TSPC) logic [Yua89]. Figure 4-6 contains a schematic of the TSPC latch. Simulations indicate that this latch can operate up to ~ 2 GHz for the chosen device sizes. All of the devices for the SCL and TSPC dividers shown in Figure 4-1 and Figure 4-6 are implemented with a channel length of 0.25 μm, whereas the channel widths are given in Table 4-1.

Table 4-1 Transistor sizing for 0.25-μm 128:1 frequency divider

SCL 8:1 Divider			
Transistors	First 2:1	Second 2:1	Third 2:1
W_1, W_2, W_{11}, W_{12}	12 μm	3 μm	3 μm
W_3, W_4, W_{13}, W_{14}	6 μm	6 μm	6 μm
W_5, W_6, W_{15}, W_{16}	2.1 μm	2.1 μm	4.2 μm
W_7, W_8, W_9, W_{10}	5.1 μm	2.55 μm	2.55 μm
TSPC 16:1 Divider Sizes Are Same for each 2:1 TSPC Divider			
W_2, W_3, W_4, W_5, W_6, W_7, W_8, W_{10}		6 μm	
W_1, W_{11}		3 μm	
W_9		12 μm	

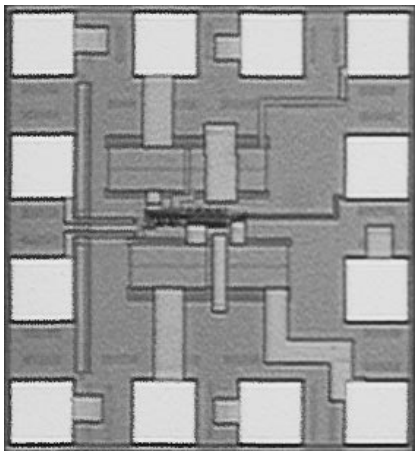


Figure 4-7 Die photograph of 0.25-μm, 128:1, 10-GHz source-coupled divider.

Figure 4-7 shows a die photograph of the 128:1 divider [Flo00a]. The die size is 730x510 μm^2. On-chip 20-pF bypass capacitors are included between V_{dd} and ground for the 8:1 SCL divider, 16:1 TSPC divider, and output buffer. Separate supplies are used for each circuit to prevent any low-frequency supply noise from the latter stages of the divider from corrupting the high-frequency operation of the first 8:1 divider. In particular, when

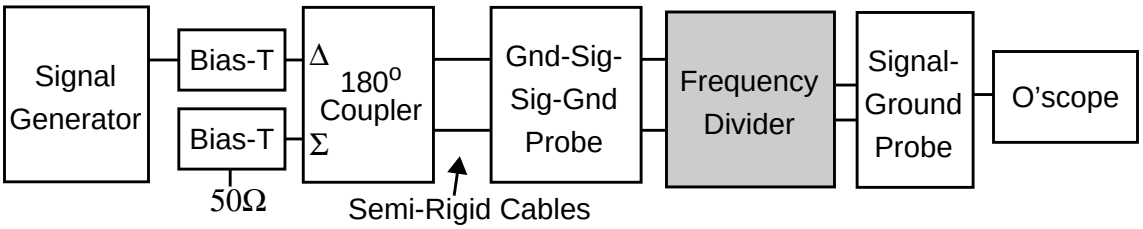


Figure 4-8 Measurement setup used to characterize dual-phase frequency divider.

the output buffer switches its 50-Ω load, a large current spike results, which can then cause the supply voltages to ring with a long time constant. In addition to the bypass capacitors, 50-Ω resistors are included between the two inputs of the 128:1 divider to ground. Since the input impedance of the divider is capacitive, and the source is 50 Ω, a reflection coefficient with magnitude of 1 results. This causes the input voltage to be twice as large as that applied by the source, potentially damaging the input transistors.

4.4.2 Measured Results

A measurement setup has been developed to characterize the divider on-wafer, and is shown in Figure 4-8. This setup consists of an external signal generator followed by a 180^o coupler, which acts as a balun. Thus, the unbalanced signal from the sweeper is converted to differential input signals for the divider whose power is (ideally) 3 dB less than the power at the input of the balun. To set the common-mode voltage for the input signals, bias-Ts are placed on the differential and common-mode inputs for the 180^o coupler. This is preferable to placing the bias-Ts on the output of the coupler since phase mismatch in the bias-Ts will be eliminated. Semi-rigid cables are then used to connect the balun to the ground-signal-signal-ground probe. Finally, the divider is probed and the output is measured using an oscilloscope. A key requirement for this measurement setup is that the

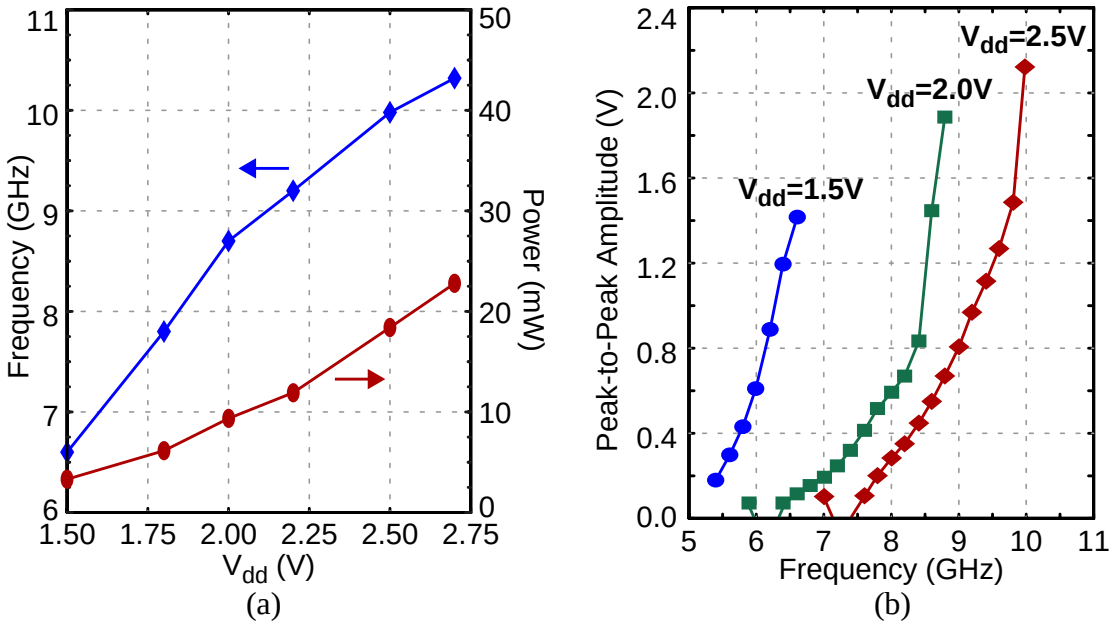


Figure 4-9 Measured results for 0.25-µm divider: (a) Maximum input frequency and power consumption versus supply voltage. (b) Input sensitivity versus frequency versus supply voltage.

phase difference between the two input signals has to be as close to 180^{o} as possible, else the divider will not operate up to its maximum operating frequency.

The measured maximum input frequency versus supply voltage for the 128:1 divider is shown in Figure 4-9(a). Also shown is the measured power consumption versus supply voltage for the 8:1 divider core. At a 2.5-V supply, the 8:1 divider operates up to 9.98 GHz, while consuming 18.4 mW. The measured output waveform for a 9.98-GHz input signal is shown in Figure 4-10. The reduced output swing is due to driving a 50-Ω output load. At 1.5 V, the divider can operate up to ~6.6 GHz while consuming 3.3 mW. These are excellent speed and power trade-offs for a 0.25-µm technology.

To measure the input sensitivity of the divider, the minimum input power level for each input frequency was recorded for multiple supply voltages. Figure 4-9(b) shows the resultant plots. For a 2.5-V supply, a 2.2-V_{pk-pk} input signal is required to operate at the

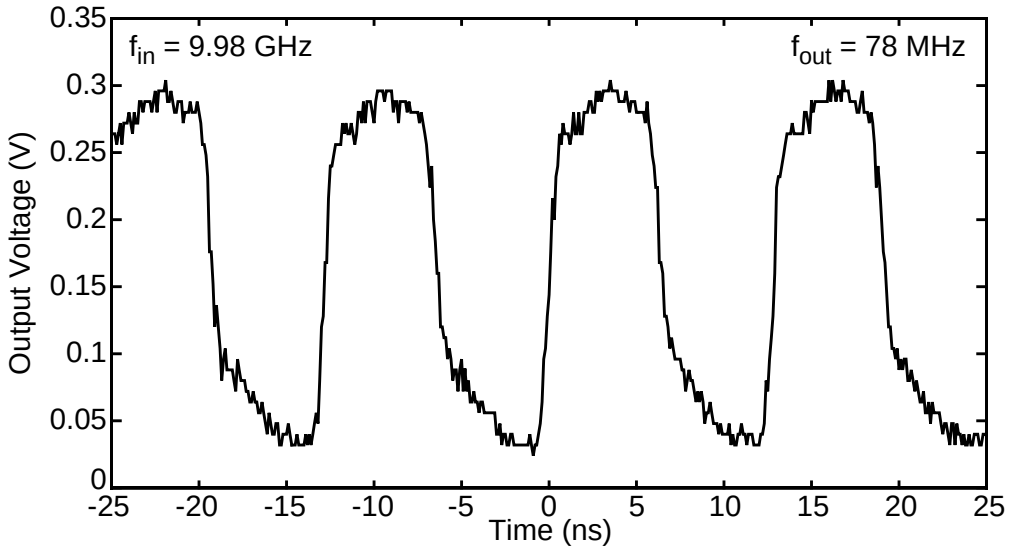


Figure 4-10 Measured output waveform from 0.25-µm CMOS 128:1 frequency divider. Input frequency is 9.98 GHz for V_{dd} = 2.5 V and output frequency is 78 MHz.

maximum input frequency of 10 GHz. This input swing is almost equal to the supply voltage; thus, the MDS of the receiver for this frequency would be very high. However, if the input frequency is decreased to 7.4 GHz, then only a ~40-mV_{pk-pk} input signal is required, directly corresponding to an improvement in the receiver MDS. The measurements shown in Figure 4-9(b) were not obtained at very low frequencies; thus, the characteristic input sensitivity plot, as shown in Figure 4-4(a) was not completely obtained. Specifically, for frequencies below f_{iSO}, the required input voltage swing should increase. This trend is only beginning to be evident for the 2.0-V and 2.5-V plots in Figure 4-9(b). The f_{iSO}'s are approximately 6.1 and 7.3 GHz for V_{dd} = 2.0 and 2.5 V, respectively. These numbers do not agree well with the simulated values from SPICE, due to an inconsistency between the simulated transistor model capacitance and the model capacitance fit to the actual wafer data. Table 4-2 summarizes the measured results for the 0.25-µm frequency divider.

Table 4-2 Summary of measured characteristics for SCL frequency dividers

Frequency Divider	0.25-µm Divider	0.18-µm Divider
Division Ratio	128:1	64:1
f_{max}	6.6 GHz @ 1.5 V 8.8 GHz @ 2.0 V 9.98 GHz @ 2.5 V	15.8 GHz @ 1.5 V 20.4 GHz @ 2.1 V
f_{iSO}	6.1 GHz @ 2.0 V 7.3 GHz @ 2.5 V	9.15 GHz @ 1.5 V 14.2 GHz @ 2.1 V
Power	3.3 mW @ 1.5 V 9.4 mW @ 2.0 V 18.4 mW @ 2.5 V	4.5 mW @ 1.5 V 12.2 mW @ 2.1 V

4.5 A 15.8-GHz, 0.18-µm CMOS SCL Divider

4.5.1 Circuit Implementation

Building on the results achieved in the 0.25-µm CMOS technology, a 15.8-GHz 64:1 source-coupled frequency divider was implemented using a 0.18-µm CMOS technology with six layers of copper interconnects [Flo01a]. This technology was obtained from UMC as part of the SRC Copper Design Challenge, sponsored by the Semiconductor Research Corporation (SRC), Novellus, SpeedFam-IPEC, and UMC. The block diagram shown in Figure 4-11 is similar to that in Figure 4-5, except the division ratio is now 64:1 and there are two TSPC low-frequency 8:1 dividers in opposite phase. This is done to provide two output signals for testing and triggering, as well as to minimize the supply-line bounce. All of the devices for the SCL and TSPC dividers shown in Figures 4-1 and 4-6 are implemented with channel lengths of 0.18 µm and channel widths given in Table 4-3.

Figure 4-12 shows a die photograph of the 64:1 divider, with a die size of 370x590 μm^2. On-chip 20-pF bypass capacitors are included between V_{dd} and ground for the 8:1

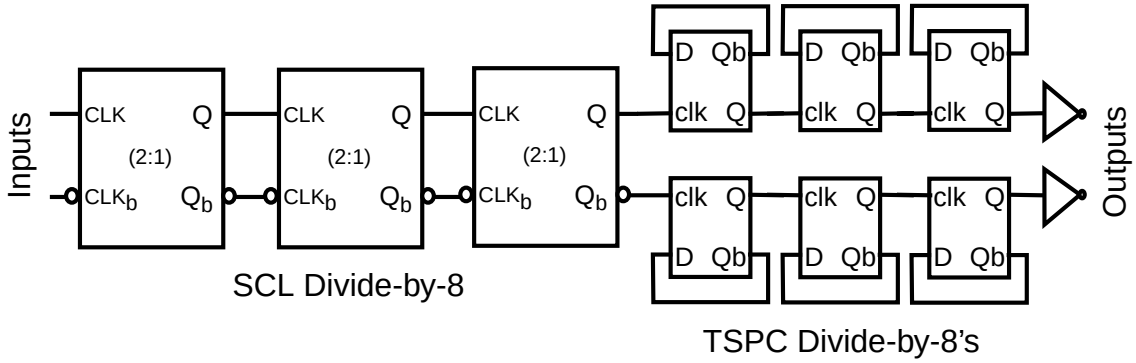


Figure 4-11 Block diagram of 64:1 divider implemented in 0.18-µm CMOS technology.

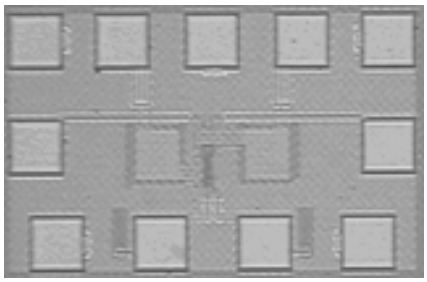


Figure 4-12 Die photograph of 0.18-µm, 64:1, 15.8-GHz source-coupled divider.

Table 4-3 Transistor sizing for 0.18-µm 64:1 frequency divider

SCL 8:1 Divider			
Transistors	First 2:1	Second 2:1	Third 2:1
W_1, W_2, W_{11}, W_{12}	7 µm	1.94 µm	1.2 µm
W_3, W_4, W_{13}, W_{14}	5 µm	3 µm	2.4 µm
W_5, W_6, W_{15}, W_{16}	1.5 µm	1.7 µm	1.5 µm
W_7, W_8, W_9, W_{10}	2.6 µm	1.2 µm	0.94 µm
TSPC 8:1 Divider Sizes Are Same for each 2:1 TSPC Divider			
W_2, W_3, W_4, W_5, W_6, W_7, W_8, W_{10}		2 µm	
W_1, W_{11}		1 µm	
W_9		4 µm	

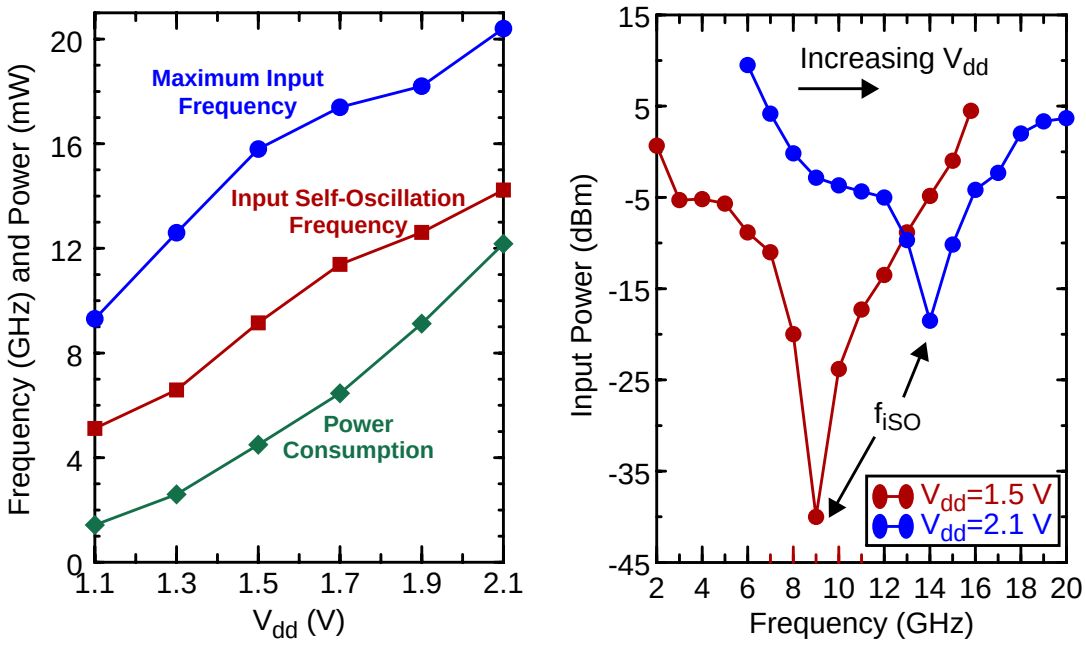


Figure 4-13 Measured results of 0.18-µm frequency divider
(a) Maximum input frequency and self-oscillation frequency versus V_{dd}.
(b) Input sensitivity versus frequency for V_{dd}=1.5 and 2.1 V.

SCL divider, 8:1 TSPC dividers, and output buffer. Again, separate supplies are used for the SCL and TSPC dividers to prevent any low-frequency supply noise from the latter stages of the divider from corrupting the high-frequency operation of the first 8:1 divider. Also, 50-Ω resistors are included between the two inputs of the 64:1 divider to ground.

4.5.2 Measured Results

Using the measurement setup in Figure 4-8, the maximum input frequency and power consumption (for 8:1 divider core) versus supply voltage plots for the 64:1 divider were obtained, and are shown in Figure 4-13(a). For a 1.5-V V_{dd}, the maximum input frequency is 15.8 GHz, and the power consumption is 4.5 mW. The maximum input frequency increases to 20.4 GHz when V_{dd} is increased to 2.1 V, while the power consumption increases to 12.2 mW. These are excellent power/speed trade-offs. Figure 4-14 shows the output waveforms for f_{in} = 15.8 and 20.4 GHz, at V_{dd} = 1.5 and 2.1 V,

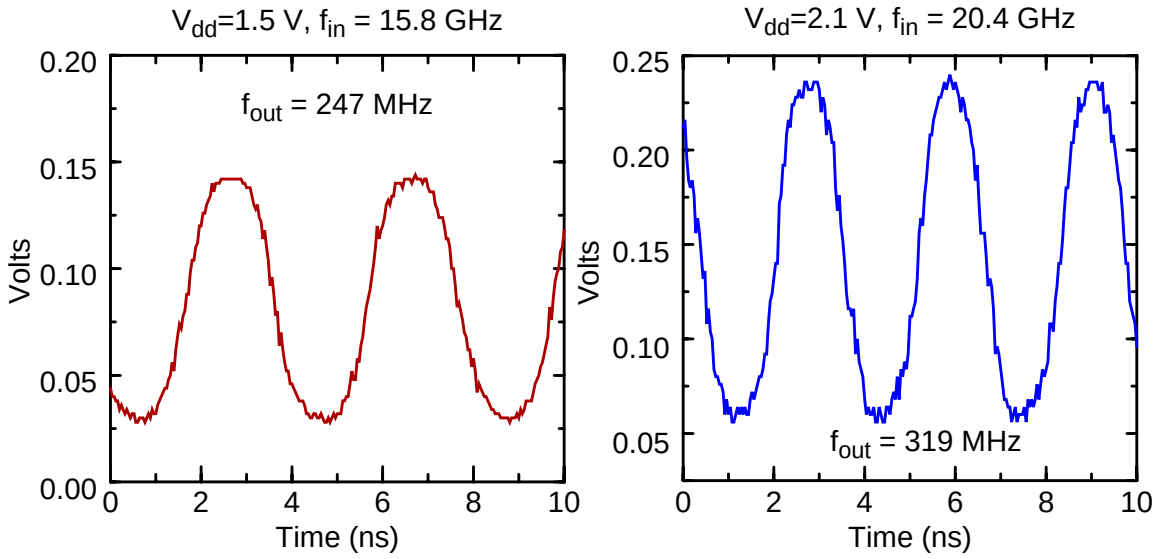


Figure 4-14 Measured output waveforms of 0.18-µm 64:1 frequency divider.

respectively. The output frequencies are 247 and 319 MHz, respectively. Once again, the reduced output swing is from driving a 50-Ω output load.

The f_{iSO} is plotted in Figure 4-13(a) versus supply voltage. At 1.5 V, f_{iSO} is 9.1 GHz, while at 2.1 V, f_{iSO} is 14.2 GHz. It can be seen that the difference between the maximum operating frequency and f_{iSO} is ~ 6 GHz. Figure 4-13(b) shows the input sensitivity for the 64:1 divider. The input sensitivity dips at the self-resonance frequency, as expected. From the self-oscillation frequency at V_{dd}=1.5 V, τ_{pd} is extracted to be 55 ps/DFF. Table 4-2 summarizes the measured results for the 0.18-µm frequency divider.

4.6 Programmable Frequency Divider Using SCL

4.6.1 Motivation and General Concept

As will be discussed in Chapter 5, a fundamental requirement for a wireless clock distribution system is ensuring that all of the clock receivers distributed throughout the chip are synchronized. This means that the delay mismatch, caused by differences in

propagation delays, of the clock signals has to be under a certain tolerance (typically less than 5-10% of a clock cycle). The difference has a *static* or time-invariant component resulting in clock skew and a *dynamic* or time-variant component resulting in clock jitter.

For the wireless clock distribution system, the static skew has both *random* and *systematic* components. Random clock skew is that which is not known *a priori*, due to gain and phase differences amongst receivers. These differences will be caused primarily by process variation and temperature gradients. Also, currently lumped into the random category are differences in the antenna gain, phase, and impedance, due to metal structure interference effects [Yoo00, Kim00b]. Note, however, that as both the antenna and system electromagnetic modeling become more robust and accurate, this skew will shift from random to systematic skew.

Systematic clock skew is caused by differences in flight times of the electromagnetic wave between the transmitter and receivers. Referring to Figure 1-2(a) for a intra-chip wireless clock distribution system, the difference in path lengths between the receivers nearest and farthest from the antennas can be a significant portion of the chip's linear dimension. For example, for a 25 x 25-mm^2 chip with an evenly distributed grid of 16 receivers, the maximum path-length difference is ~9 mm. At 15 GHz, this is close to the global clock signal's wavelength in silicon-dioxide (10.1 mm) and about 1.5 times the wavelength in silicon (5.8 mm), causing a significant phase mismatch. For an inter-chip distribution system, the path lengths will be much more equalized, which is a benefit over the intra-chip distribution system.

One method to remove the systematic skew is to ensure that the global clock signals have the same phase at each receiving antenna. This can be accomplished by forcing

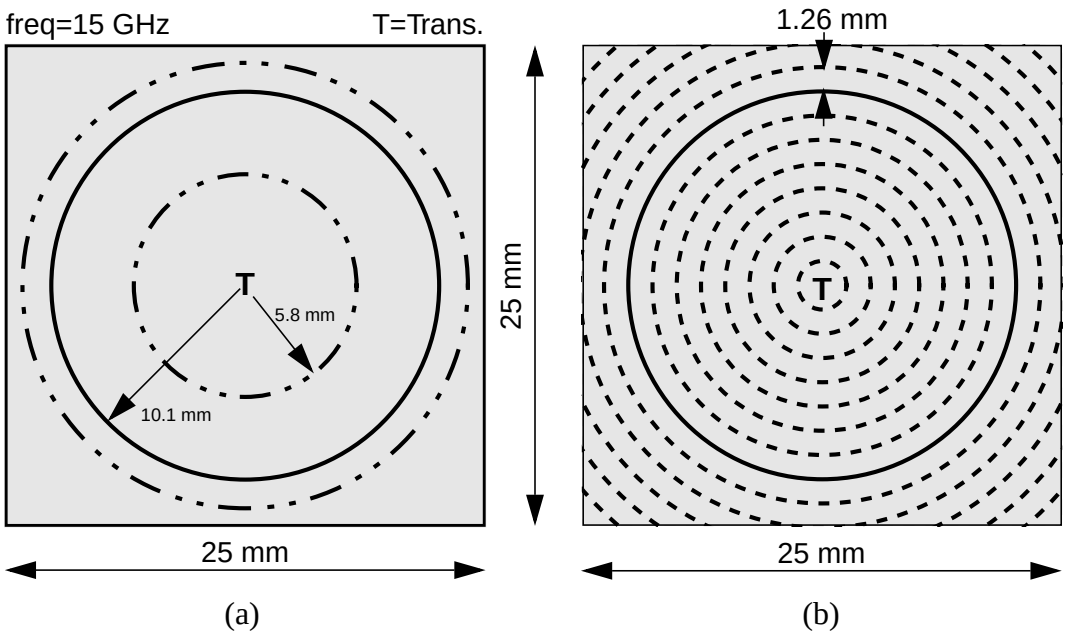


Figure 4-15 Illustrations (to scale) of grids upon which clock receivers should be placed. (a) Grid spacing of one wavelength from transmitter, with solid for wavelength in silicon dioxide and dash-dot for wavelength in silicon. (b) Grid spacing of one eighth of a wavelength in oxide, used when the dividers are programmed to initial states of 0 to 7 (for divide-by-8).

all of the receivers to be a multiple of a wavelength away from the transmitter. This concept is illustrated (to scale) in Figure 4-15(a), which shows circular grids spaced multiple wavelengths from the transmitter. The solid line represents wavelength in silicon dioxide and the dash-dotted line represents wavelength in silicon substrate. This begs the question, though, of in which medium does the electromagnetic wave propagate. Also, multipath effects will be anisotropic; therefore, the wavelength in one direction will not necessarily be the same as the wavelength in another direction. These issues will be addressed further in chapter 6. Assuming, however, that the wavelengths are known *a priori*, then the receivers can be placed on such a grid.

From examining Figure 4-15(a), it can be seen that the grid is not dense enough to accommodate clock receivers in a feasible arrangement. This is where the concept of programming or initializing the frequency divider is useful. Frequency dividers are basically

counters, where the division ratio is equal to the count (e.g., an 8:1 divider counts from 0 to 3 while outputting a one and from 4 to 7 while outputting a zero). If receivers close to the transmitter are initialized to a smaller count, and receivers far from the transmitter are initialized to a larger count, the mismatch in time-of-flight delays among the receivers will tend to be cancelled. Graphically, this reduces the grid spacing by the division ratio. Hence, for an 8:1 divider, the receivers can be placed on a grid with spacing $\lambda/8$, which then equalizes the time-of-flight delays and decreases the systematic skew to 0. This is illustrated in Figure 4-15(b), which shows the grid for wavelength in silicon-dioxide.

Since random clock skew also exists, it is impossible to design a grid to equalize the total skew. However, assuming that the total skew in the system can be estimated or detected, then the start-up state of the divider can be modified accordingly. Therefore, the worst-case total skew percentage then becomes $\pm\frac{1}{2M}$, where M is the division ratio of the divider. For an 8:1 programmable divider, the maximum output skew is +/-6.25%. Note, that if the skew can be estimated, then the receivers do not have to be placed on a grid.

The initialization methodology is conceptually illustrated in Figure 4-16, which shows two clock receivers with an initial skew of 20%. Also shown are the 8 possible start-up states/phases for the 8:1 dividers in the clock receiver. As can be seen, by selecting the correct states for each divider (requiring initial skew estimation or detection), the skew can be reduced from 20% to 3% (for this particular example).

Therefore, circuits are required to initialize the SCL divider, and a methodology is needed to start-up the clock distribution system in phase. This is complicated by the fact that the SCL dividers will self-oscillate in the absence of an input signal. Therefore, a way is needed to prevent these circuits from self-oscillating during initialization as well.

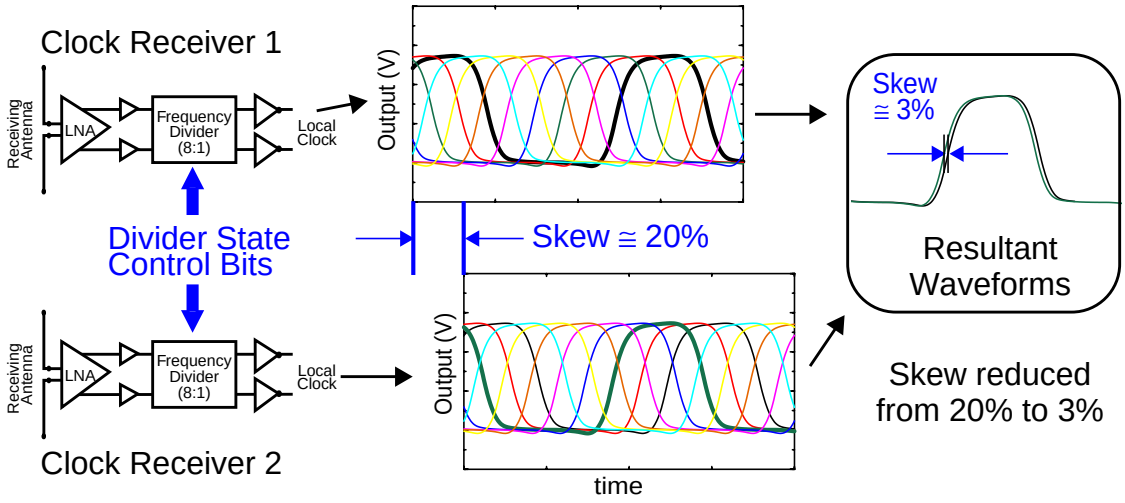


Figure 4-16 Illustrations of concept of divider programming to reduce systematic skew. Two receiver start with a skew of 20% and by selecting the correct state of each, the skew can be reduced to 3% (for this example).

Finally, the initialization circuitry should not load down the divider, which would lower the maximum frequency and change the conversion gain versus frequency.

4.6.2 System Start-Up Methodology

It has been shown conceptually how programmable frequency dividers can be used to reduce and potentially eliminate systematic clock skew. These programmable dividers will rely on some initialization signal (INI) which will denote whether the divider is to be initialized or to operate freely. Therefore, a start-up methodology is needed for the system to initialize all of the receivers to the correct state or count (CNT), and then to release these receivers from the initialized state to the free-running state.

For programming the dividers, there are two basic methods--dynamic and static. One is to correct the system dynamically with feedback. Here, the phase-offset between each clock receiver and its nearest neighbors can be measured with a phase detector, and then the CNT of the dividers can be adjusted accordingly. The system is basically

operating as a delay-locked loop (e.g., [Sut95]), where the phase of all of the receivers will be dynamically adjusted to a steady-state phase lock. This system is very similar to a distributed synchronous clocking approach [Pra95]. The benefit of this system is that very small skew can be obtained, equalizing both random and systematic phase errors. Also, phase errors will not accumulate, since the system is controlled dynamically. However, distributed synchronous clocking eliminates the need for integrated antennas and wireless interconnects. Instead, multiple independent oscillators can be distributed throughout the chip, and then phase-locked to one another, as in [Gut00]. Distributed clocking has the following disadvantages, though: the benefit of having another communication medium on chip is eliminated; jitter will spread and accumulate across the chip, since phase noise from each input signal is transferred through the phase-locked loops via low-pass filter responses; and there is added complexity to the system.

A second option for programming the dividers and starting up in a synchronized state is to train the system at start-up, detecting the phase error for each receiver. Here, the receiver phase errors are detected during training and a CNT value is extracted. The appropriate CNT values are held in memory and used during normal system operation. This phase-correction is static rather than dynamic, happening only once during system operation. This static phase correction has the drawback of accumulating phase errors. In other words, once the system is programmed, there is no other way to correct for phase errors caused by noise or system fluctuations (e.g., power line fluctuations). Therefore, the signal-to-noise ratio of the system would have to be high.

The training mode would have the following conceptual steps. First, the clock transmitter broadcasts the global clock (GCLK) used as a training signal. Second, each

clock receiver detects GCLK with INI = 0 and CNT = 0, and generates a local clock (LCLK). These LCLK's have random and systematic clock skews. Third, the skew is measured against the receiver's neighbors with phase detectors and converted to a digital word with a 3-bit analog-to-digital converter (3 bits for 8 states). Note that a method is needed to prevent mode-locking [Pra95], where systematic offsets can occur if the phase offsets from multiple receivers are simply added (i.e., offset from one receiver is $+90^{o}$ and offset from another receiver is -90^{o} resulting in a net of zero phase offset, however all of the receivers would be out of phase). To prevent mode-locking a non-monotonic phase detector response is required [Pra95]. Fourth, GCLK is turned off, and each receiver is initialized to the appropriate state, with INI = 1 and CNT = 3-bit word from previous step. Fifth, either all of the clock receivers "report" back to the transmitter when they have been initialized, or the system waits a certain amount of time for initialization to occur. Sixth, following training, GCLK is released and the receivers should begin detecting the signal and generating the synchronized LCLK's. However a method is still required to release the initialization signal once GCLK is present at the input to the frequency divider. This is complicated by the fact that the frequency divider self-oscillates without the input signals present. Approaches to synchronously release the dividers from the initialized states will be the subject of future work.

4.6.3 Circuitry for Programmable SCL Divider

The dividers used up to this point have been asynchronous, consisting of cascaded 2:1 dividers. Therefore, an initialization methodology for a 2:1 divider is required before a 2^{N}:1 divider can be initialized. Figure 4-17(a) shows a block diagram of a 2:1 divider

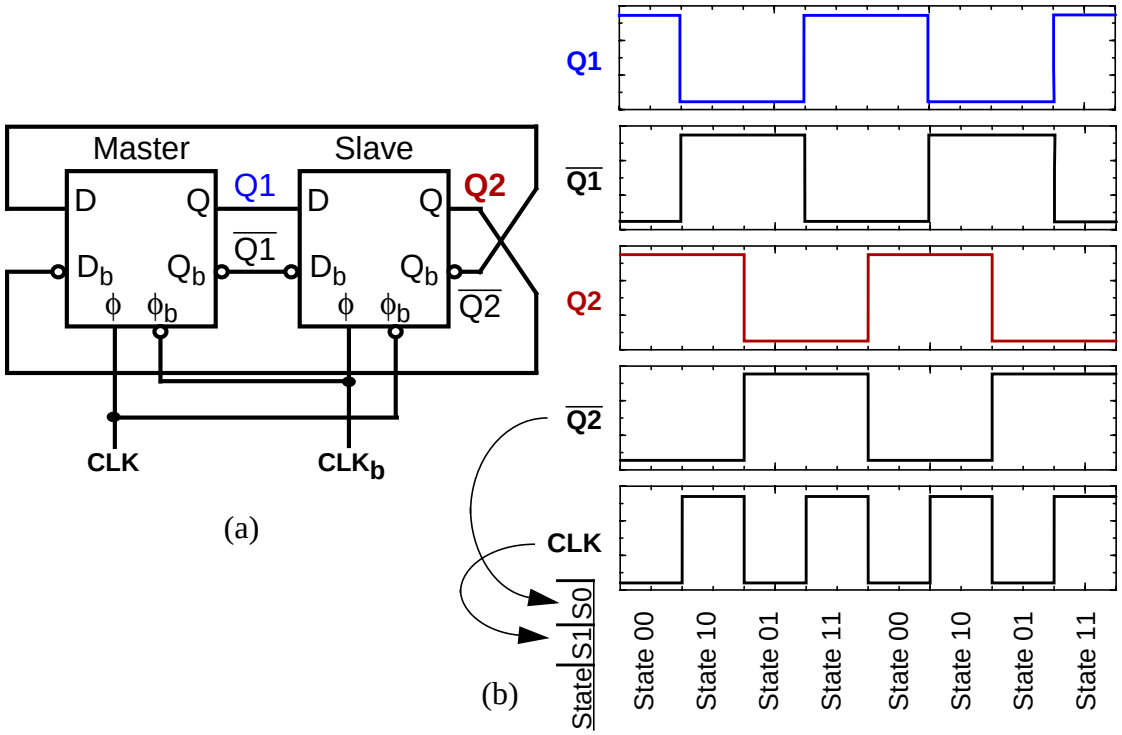


Figure 4-17 (a) Block diagram of 2:1 frequency divider using SCL and (b) ideal input and output waveforms for divider and associated states.

employing SCL. A schematic of the SCL DFFs is shown in Figure 4-1(c). Figure 4-17(b) shows ideal waveforms for the input clock signal as well as for all four of the “drain” nodes in the divider, labelled Q1, $\overline{Q1}$, Q2, and $\overline{Q2}$. Examining these waveforms, it can be seen that the divider has four possible states. State variables S1 and S0 are introduced to identify these states, where S1 is the desired value of the divider input (i.e., clock signal) and S0 is desired value of the divider output, defined to be $\overline{Q2}$.

The initialization circuitry should set all of the drain nodes for each of the four possible states. This results in the truth table shown in Table 4-4, which is obtained with the help of Figure 4-17(b). The drain nodes can then be defined logically by the state variables, as shown in the table. Therefore, during initialization, drain nodes Q2 and $\overline{Q2}$ are set to $\overline{S0}$ and S0, respectively, while drain nodes Q1 and $\overline{Q1}$ are set to the exclusive-nor

Table 4-4 Truth table for initialization circuitry

State		Output Drain Nodes			
S1 (Clock)	S0 (Output)	Q2	$\overline{Q2}$	Q1	$\overline{Q1}$
0	0	1	0	1	0
1	0	1	0	0	1
0	1	0	1	0	1
1	1	0	1	1	0
Logic Function:		$Q2 = \overline{S0}$	$\overline{Q2} = S0$	$Q1 = \overline{S1 \oplus S0}$	$\overline{Q1} = S1 \oplus S0$

and exclusive-or of S1 and S0, respectively. When not in initialization, these drain nodes should be unmodified both in terms of their logic value and in terms of their impedance, allowing the divider to operate at full speed.

The schematic of the 2:1 divider with the initialization circuitry is shown in Figure 4-18. This circuitry meets all of the above requirements. The multiplexed initialization data is introduced through PMOS transistors $M_{7,8}$, which inverts the data. Therefore, the logic functions for the PMOS gate inputs are as follows:

$$V_a = \overline{S1 \oplus S0} \cdot INI, \tag{4.6}$$

$$V_b = S1 \oplus S0 \cdot INI, \tag{4.7}$$

$$V_c = \overline{S0} \cdot INI, \tag{4.8}$$

$$V_d = S0 \cdot INI. \tag{4.9}$$

The drain nodes are the inverse of these functions. Since PMOS transistors will only be able to pull the drain nodes high when their inputs are low. Therefore, very weak NMOS transistors (M_9) are included to activate the regenerative pairs ($M_{5,6}$) when INI = 1. When

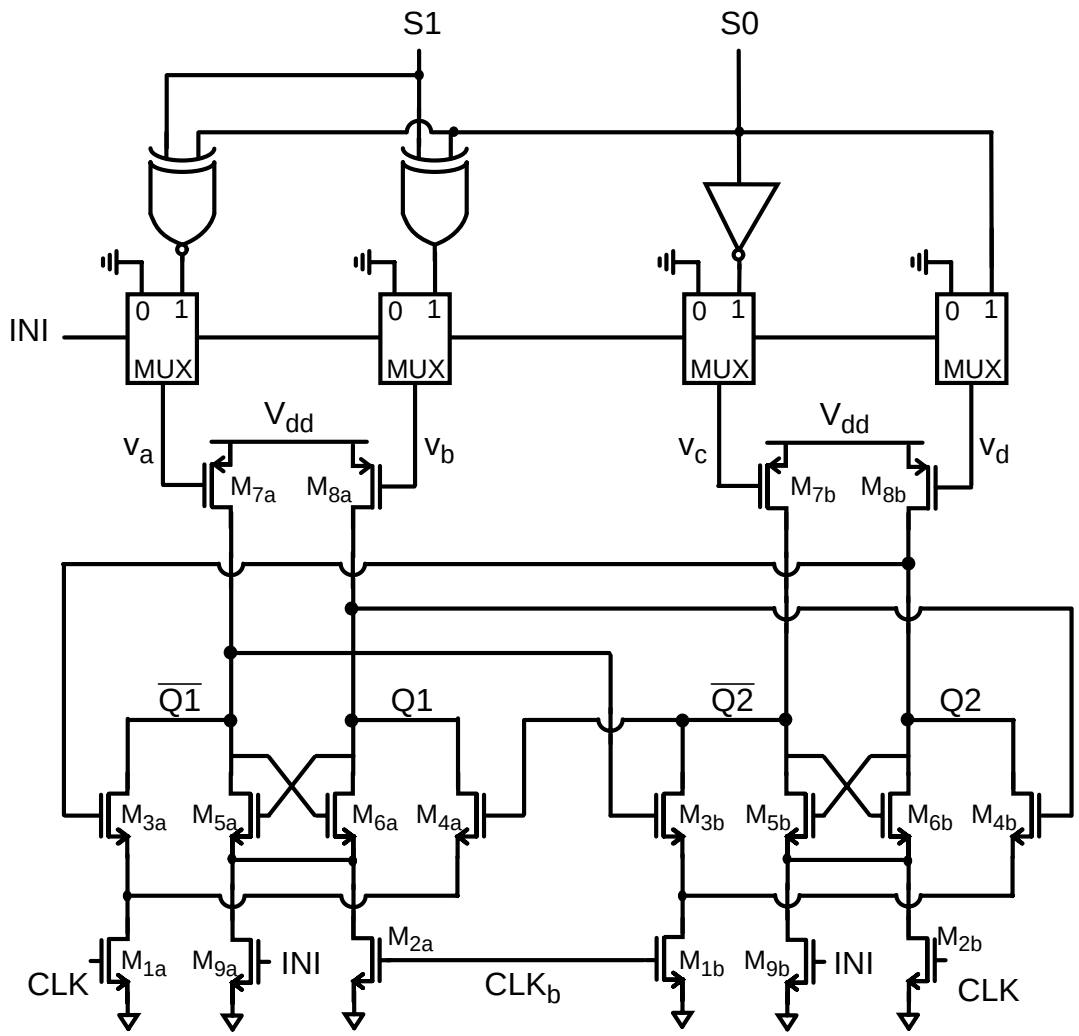


Figure 4-18 Schematic of 2:1 frequency divider with initialization circuitry.

one of the PMOS transistors pulls its drain up to V_{dd}, the positive feedback in the regenerative pair causes the other drain to be pulled down to ground. Since these PMOS transistors originally had their gates grounded to act as pseudo-NMOS loads, the initialization data are multiplexed with a ground signal, where the INI signal controls the multiplexer. Thus, for INI = 1, V_x is defined as above, and for INI = 0, $V_x = 0$.

The logic blocks are implemented using complimentary pass-transistor logic (CPL) [Bel95], in a logic array. Inputs to the array, shown in Figure 4-19, are S1, S0, INI, and their complements. Inverters are required at the output of each logic function to

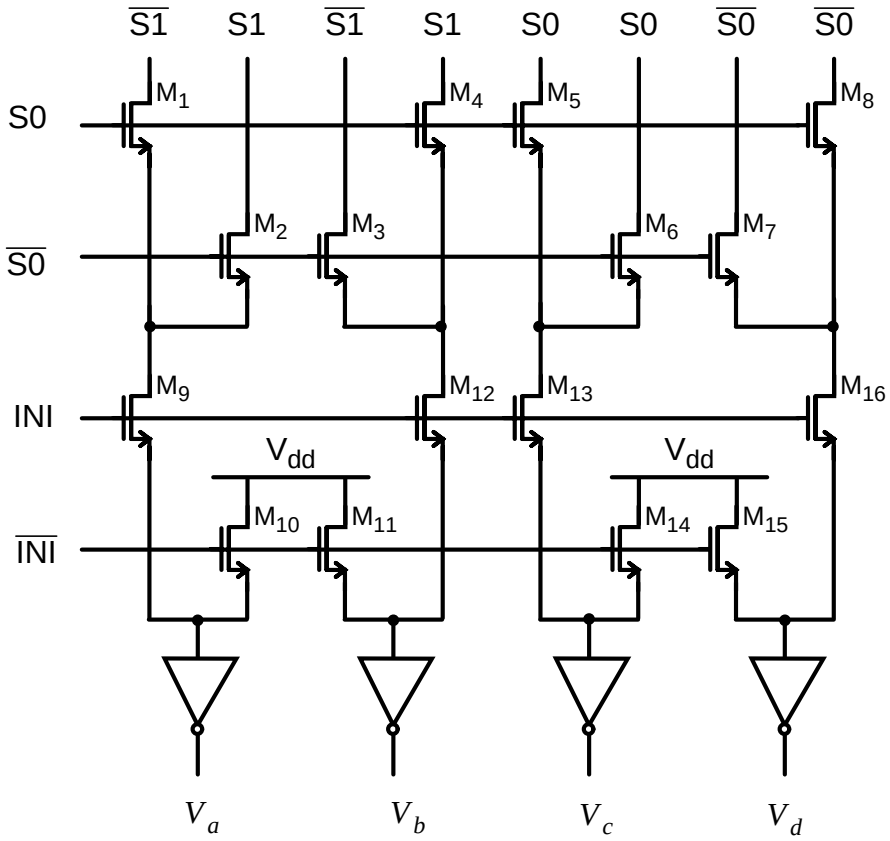


Figure 4-19 Schematic of initialization circuitry implemented with complementary pass-transistor logic.

restore the voltage levels. A benefit of CPL is that only NMOS transistors are used for the logic array, allowing for very compact layout.

Finally, to realize the 8:1 programmable divider, three 2:1 programmable dividers are cascaded. Since the state-control inputs S1 and S0 are the desired input and output values of each 2:1 divider, then S0 for the first 2:1 divider is equal to S1 for the second 2:1 divider, and S0 for the second 2:1 divider is equal to S1 for the third 2:1 divider. The resultant 8:1 divider block diagram is shown in Figure 4-20. Input S1 for the first 2:1 divider is set to ground, since simulations show that a total of only eight states rather than sixteen are possible for this divider (i.e., S1 = 0 yields 8 states and S1 = 1 yields the same 8 states). State control inputs $X_2X_1X_0$ form a binary number equal to the desired count

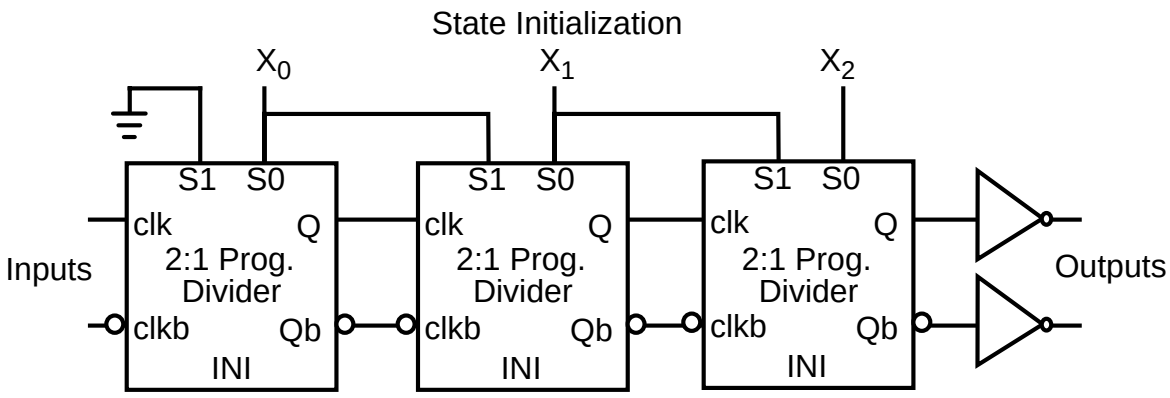


Figure 4-20 Block diagram of programmable 8:1 frequency divider

(CNT) of the divider (i.e., decimal 0-7). This CNT will come from the 3-bit A/D converter after the phase detector.

4.6.4 Simulated Results

Basic functionality of the initialization circuit is demonstrated in Figure 4-21, which shows the simulation results for an 8:1 divider for $X_2X_1X_0$ ranging from binary #000 to #111. As can be seen, the output phase can be varied in increments of $\pi/4$ ($2\pi/M$) or 45^o. This simulation was performed under identical conditions for each state. Thus, the divider was initialized at time zero, and then after a certain delay the INI signal was released along with the input clock signals.

There is an inherent flaw, however, in the implementation of this programmable divider which subsequent measurement results revealed. The failure surfaced when attempting to repeatedly initialize the divider to the same CNT. When the divider had already been running and then INI was invoked and then released, the divider would initialize to any of the eight possible states. This means that the actual initialized value for a given CNT depends on the current state of the divider when INI transitions high.

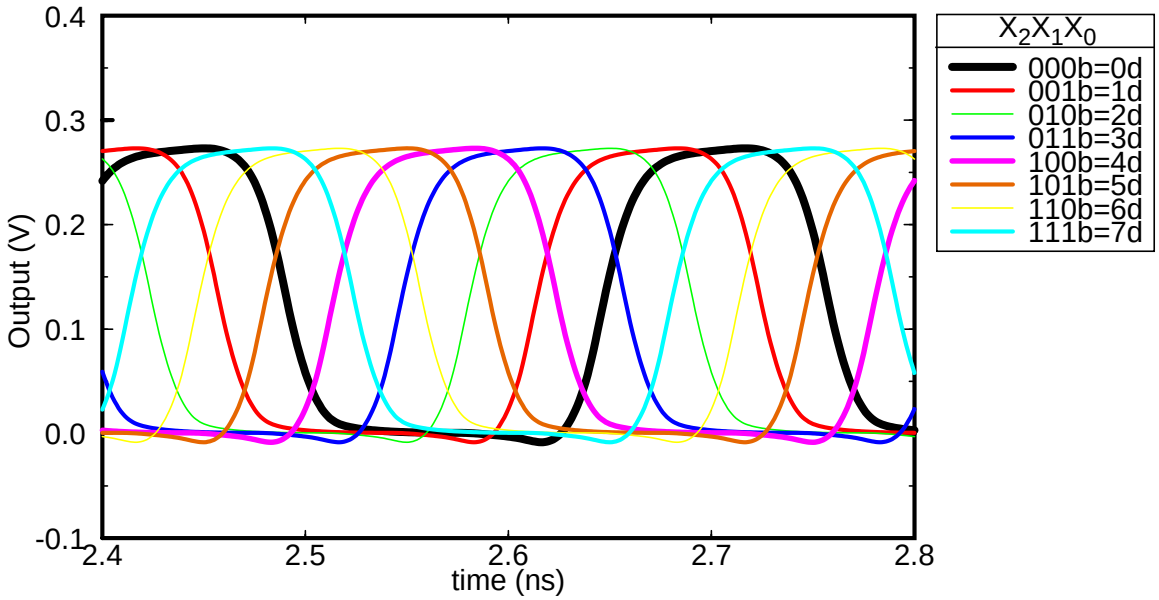


Figure 4-21 Output waveforms of 8:1 divider for each start-up condition

This effect can be demonstrated and analyzed using SPICE. Figure 4-22 shows the simulated signals for two programmable 8:1 dividers operating at an input frequency of 30 GHz. In this simulation, the clock signals are always present, and the INI signal is being switched repeatedly from high to low, as indicated in the plots. One divider is always initialized to CNT = #000, while the other divider is always initialized to CNT = #111. Ideally, this should correspond to a phase offset of 45^{o} between the two dividers each time the divider is initialized. As can be seen from Figure 4-22, after the first two initializations, the output waveforms take the desired 45^{o} difference. However, after the third initialization, the output phase difference is 90^{o}. The failure of the circuit can be seen by examining the output waveforms from the first, second, and third 2:1 dividers (referred to as the 2:1, 4:1, and 8:1 outputs). Since one divider is initialized to state #000 and the other is initialized to state #111, each time INI = 1, the 2:1, 4:1, and 8:1 outputs should be all zeros or all ones, for the #000-divider and #111-divider, respectively. From the waveforms in Figure 4-22,

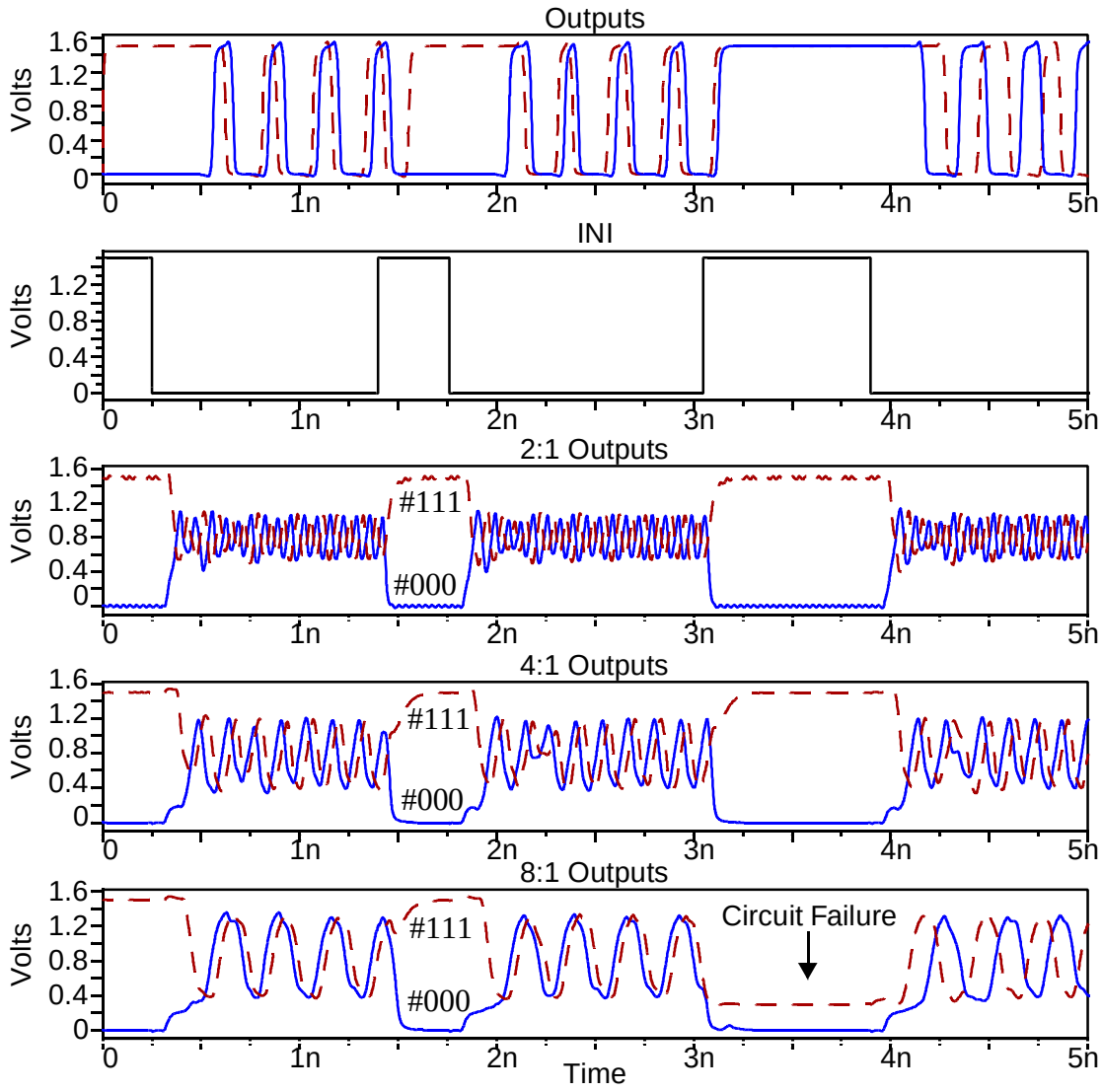


Figure 4-22 Simulated waveforms of two programmable 8:1 dividers--programmed to #000 (solid lines) and #111 (dashed lines)--for repeated initializations. On the third initialization the circuit fails, as indicated.

during the third initialization, the 8:1 output of the #111-divider stays low, changing the programmed state from #111 to #110. This accounts for the extra 45^{o} phase shift.

Depending on the state that each 2:1 divider is in when INI transitions high, the circuit may not initialize to the correct state. Figure 4-23(a) shows plots of the drain voltages for the third 2:1 divider (i.e., 8:1 outputs) around the failure time of the third

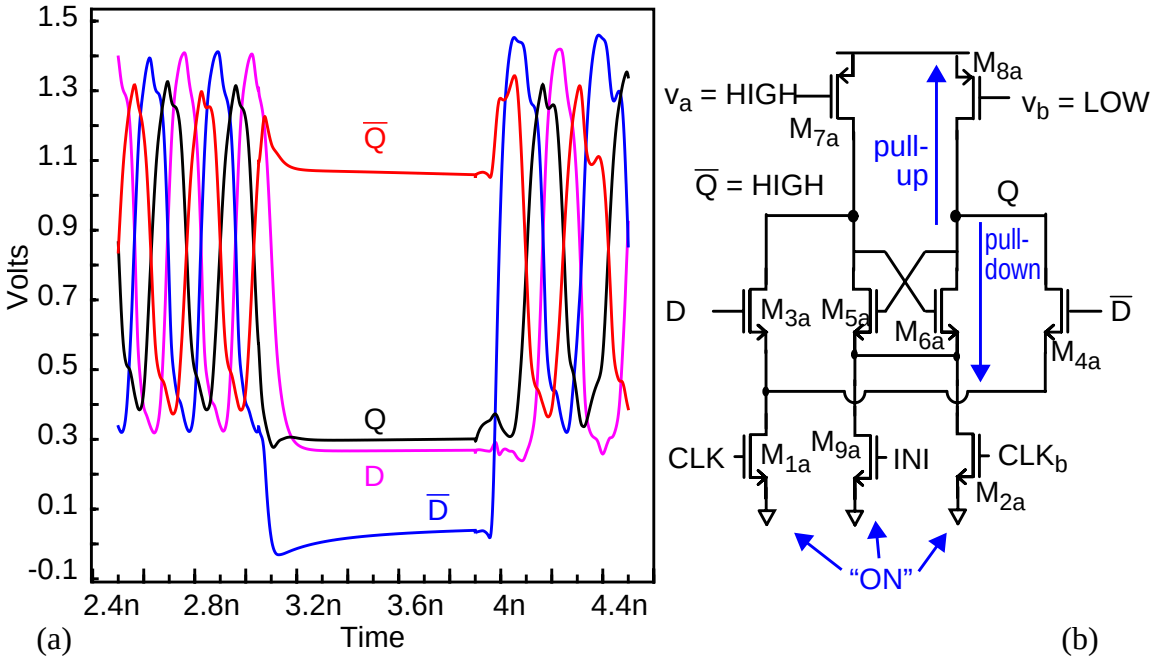


Figure 4-23 (a) Simulated waveforms of programmable 2:1 divider during state-dependent initialization failure. (b) Schematic of DFF indicating conflict of states.

initialization. These waveforms, Q, $\overline{Q}$, D, and $\overline{D}$ are identified in the schematic shown in Figure 4-23(b). The desired states of Q and $\overline{Q}$ during initialization are high and low, respectively; thus, V_b and V_a are 0 and 1, respectively. For Q to be high during initialization, it has to be pulled up through M_{8a} with V_b low. However, depending on the values of $\overline{Q}$ and $\overline{D}$, there will also be a discharge path to ground for Q. The pull-down paths are possible since $M_{1a,2a,9a}$ are all on. As seen in Figure 4-23(a), $\overline{Q}$ is ~1.1 V; thus, the pull-down path through M_{6a} is quite strong. The actual value of Q1 is set through a voltage divider, with the value depending on the current state of the divider when INI switches high.

To rectify this problem, both the evaluate and hold portions of the DFF should be turned off when INI = 1. Also, both high and low values have to be written to the drain nodes of the divider (as opposed to the PMOS only being able to pull the node high). Figure 4-24(a) shows the new programmable DFF to be used in the 2:1 divider with these

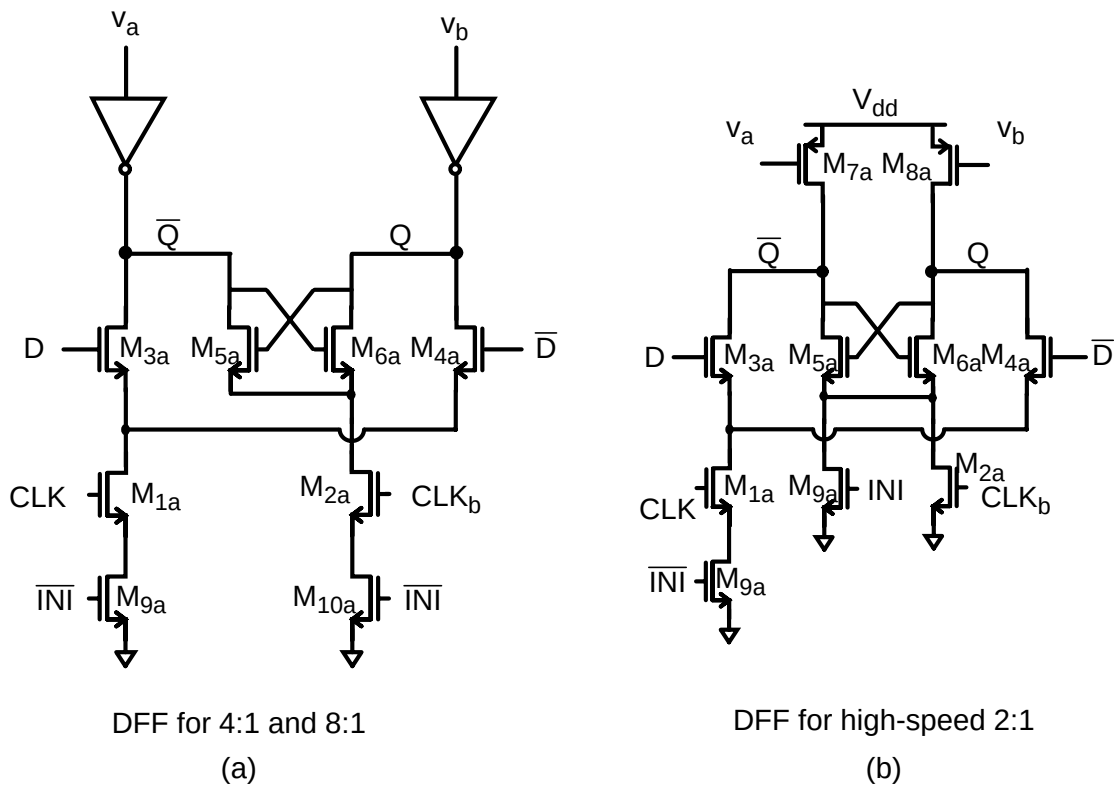


Figure 4-24 (a) Schematic of fixed programmable DFF (for lower frequency divide-by-4 and divide-by-8). (b) Schematic of improved high-frequency (divide-by-2) programmable DFF.

modifications. The evaluate and hold portions are turned off during INI=1 by including two transistors, driven by $\overline{INI}$, in series with the CLK and CLK_b transistors (performing a logical AND function). To write both high and low values to the drain nodes, the PMOS transistors are replaced with inverters. The size of the NMOS transistor in this inverter is kept small. Simulations show that using this new DFF in the lower frequency 4:1 and 8:1 stages eliminates the state-dependent initialization failure. However, using this DFF in the high-frequency 2:1 stage decreases the operating frequency, due to the increased capacitive load from the inverter. Thus, the modified DFF shown in Figure 4-24(b) is used for the first 2:1 stage. Simulations show that this stage will initialize properly due to the sizing ratio between the PMOS and NMOS. However, in future implementations of this divider,

the initialization has to be carefully checked for the first 2:1 divider, and the appropriate DFF shown in Figure 4-24(a) or (b) should be selected.

The correct operation of the programmable 8:1 divider with the new DFF's was verified in simulations. The scenario is the same as in Figure 4-22, where two dividers are programmed to CNT = #000 and #111, with INI switching from high to low repeatedly. Figure 4-25 shows the simulated results. As can be seen, each time INI goes high, the outputs of the #111-divider go high and those of the #000-divider go low. There is no longer any situation where the output nodes of the DFF's are mistakenly pulled low when they should be high. As a result, the outputs between the 8:1 dividers always maintain a 45^o phase shift. Thus, these new DFF's remove the dependence of initialization on the current state of the divider, and should allow the start-up state of the divider to be programmed in 45^o increments as originally planned.

4.6.5 Testing Methodology

A methodology is needed to characterize the clock skew between independent dividers, and to demonstrate the initialization circuitry. Measuring the clock skew between two clock circuits using wafer probing would require matching the delay through the external measurement system (probes, 3.5-mm coaxial cables, RF connectors), such that the measured clock skew is due only to the skew in the circuits themselves. However, matching these external components to within ~20% of the required skew (which is 10% of the local clock period) is a difficult task, or in other words the external components need to be matched to within 8 ps for a 2.5-GHz local clock. Therefore, the clock skew is detected on chip using a phase detector, which acts as a skew-to-voltage converter.

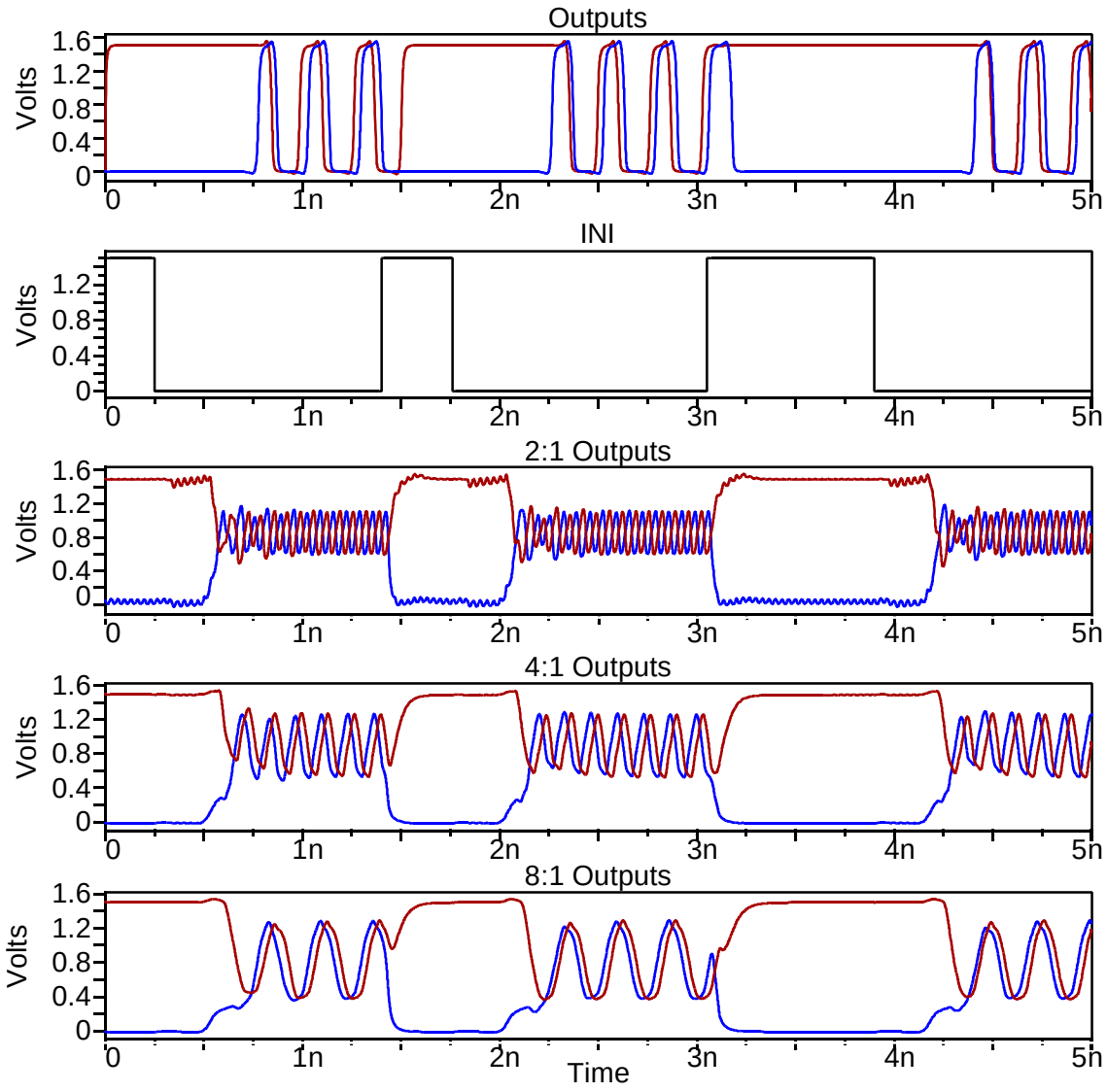


Figure 4-25 Simulated waveforms of two programmable 8:1 dividers with the new DFFs--programmed to #000 (solid lines) and #111 (dashed lines)--for repeated initializations. The circuit functions correctly and the output phase differenc between the two dividers remains constant.

Figure 4-26(a) shows a schematic of the phase detector (PD) and low-pass filter (LPF) [Raz95]. The PD functions as an exclusive NOR circuit (transistors $M_{1\text{-}6}$). A pseudo-NMOS load is used. A key feature is that this PD is symmetric for inputs CLK1 and CLK2. This eliminates any systematic phase error that would be introduced using

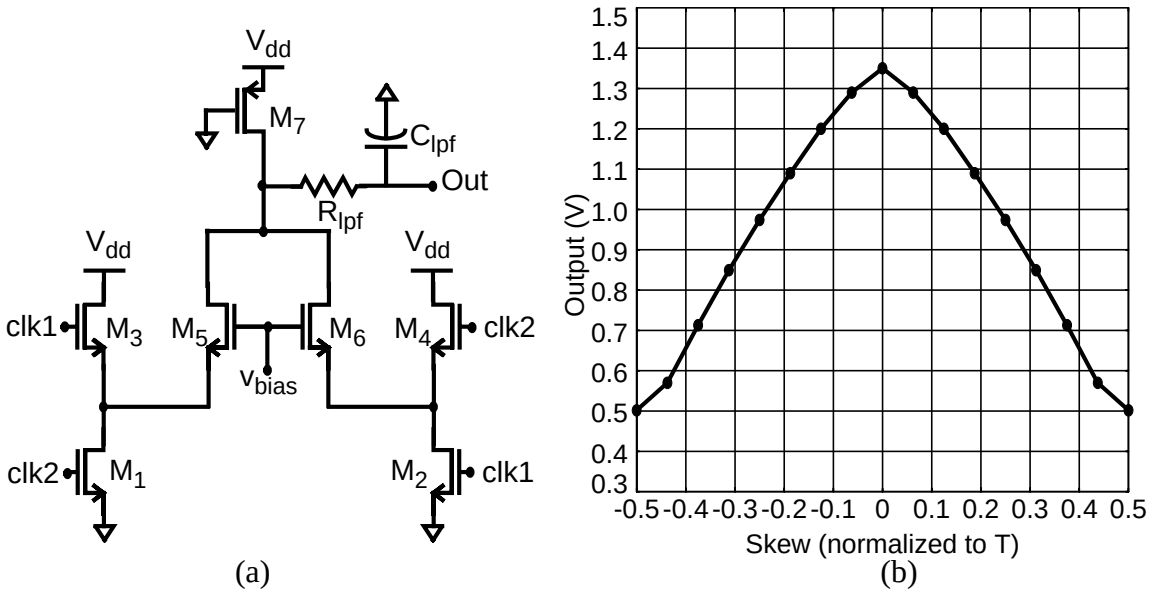


Figure 4-26 (a) Schematic of phase detector and low-pass filter (b) Output of phase detector versus input skew

conventional XOR or gilbert cell architectures. Another benefit is the use of single-ended inputs; thus, only a single-ended clock signal has to be routed to the PD. Figure 4-26(b) shows the simulated output voltage versus input clock skew for the PD and LPF. The voltage-skew plot is symmetric with respect to skew=0; hence, the absolute value of skew is measured. Since the output of the PD is close to linear, it can be characterized by measuring the output voltage for 0^o and 180^o phase offset. The measured skew can then be extrapolated based on these two data points. Note that the voltage-skew plot repeats every period, therefore, the measured clock skew will be *modulo* T_{clk} ($t_{skew\_extracted} = t_{skew}$ mod T_{clk}), where T_{clk} is the period of the local clock signal.

4.6.6 Measured Results

To evaluate the operation of the initialization circuitry, a phase-detector and a low-pass filter were implemented on-chip with two identical frequency dividers. These frequency dividers were implemented with the original DFF's (Figure 4-19) since the

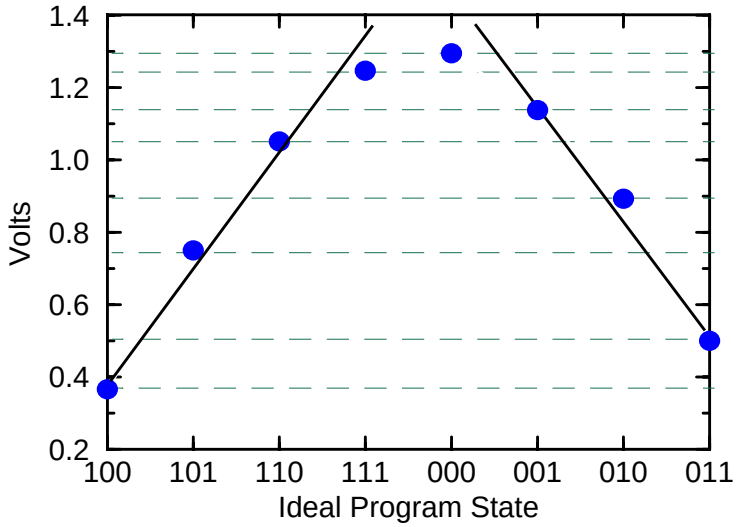


Figure 4-27 Measured outputs of phase detector used to characterize initialization circuitry.

state-dependent initialization failure had not yet been identified. One divider was always initialized to state #000, while the other divider's state was programmable. Measurements of the two-divider test structure reveal that the output phase difference between the two dividers can take on one of eight discrete values, indicating that the start-up phase of the dividers was being adjusted. These eight values are shown in Figure 4-27 versus the ideal programmed state. However, for each programmed state, the output would not take on the same phase value for multiple repetitions of the experiment (i.e., INI switching on and off). For example, when the divider was programmed to state #100, this should correspond to a 180^{o} phase difference and the output of the phase detector should be at its minimum point. However, the phase detector output would take on any of the eight possible values, since the initialized value depends on the current state of the divider. Thus, every programmable state yields any of the eight possible phase values, indicated by dotted lines in Figure 4-27. This shows that the initialization process is not working correctly, which led to the development of the new DFF's to remove this state-dependence. The fact that the

output phase-difference was quantized does verify partial operation of the circuit. It is expected (and simulations indicate) that this circuit will operate correctly when the new DFFs given in Figure 4-24 are used.

4.7 A 0.1-μm CMOS $[DP]^2$ Divider on SOI and Bulk Substrates

4.7.1 Circuit Implementation

Dividers utilizing SCL do not require or generate full-swing input and output signals. As a result, their operating speed can be higher than full-swing dividers, since it takes longer to charge a given capacitive load to a larger voltage swing using a given current (i.e., $\tau = \frac{CV}{I}$). A benefit of full-swing dividers is that they generally can be implemented with fewer transistors, and, hence, the layouts are more compact. However, in addition to their lower speed, full-swing dividers can have a reduced input sensitivity (or conversion gain) since they require larger input signals.

Full-swing dividers are commonly implemented using true-single phase clocked (TSPC) logic [Yua89] or clocked CMOS (C^2MOS) logic [Wes92]. An alternative type of high-speed logic is dual-phase dynamic pseudo-NMOS ($[DP]^2$) logic [Biy96, Yan99a]. The C^2MOS and $[DP]^2$ inverters are shown in Figures 4-28 (a) and (b), while a $[DP]^2$ DFF is shown in Figure 4-28(c). The $[DP]^2$ inverter is evolved from a C^2MOS inverter by eliminating the PMOS transistor used for logic evaluation. This reduces the input and load capacitance of the inverter, increasing the speed for a given power dissipation. Also, the removal of the PMOS transistor decreases the series resistance for charging the output node, further increasing the speed. Since all three transistors of a $[DP]^2$ inverter are on during evaluation, the pull-down action of the NMOS transistors has to be made stronger

than the pull-up action of the PMOS transistor. This is done by choosing the widths of M_{n1} and M_{n2} such that their $\mu C_{OX}\frac{W}{L}$ is approximately 4 times that of M_{p1}.

Figure 4-29 shows a schematic of a 4:1 frequency divider, employing $[DP]^2$ logic in a divide-by-2N topology. The synchronous divide-by-2N circuit is formed by placing N edge-triggered DFFs with an inverter in a loop. Each edge-triggered DFF is composed of two level-sensitive $[DP]^2$ latches with opposite clock polarities, and each $[DP]^2$ latch is simply a clocked pseudo-NMOS inverter [Biy96]. The circuit basically operates as a ripple chain, where a change at a single divider node will ripple through each stage, returning to the same node N clock-periods later with opposite polarity, taking 2N clock cycles for a full output period. The $[DP]^2$ latch delay can be extracted from the speed of the divider, since the maximum clock frequency is limited by the delays through the final $[DP]^2$ level-sensitive latch and the pseudo-NMOS inverter (which are approximately equal). Therefore, the delay through both of these will be approximately one half the minimum input clock period, and the $[DP]^2$ latch delay is then one fourth the minimum input clock

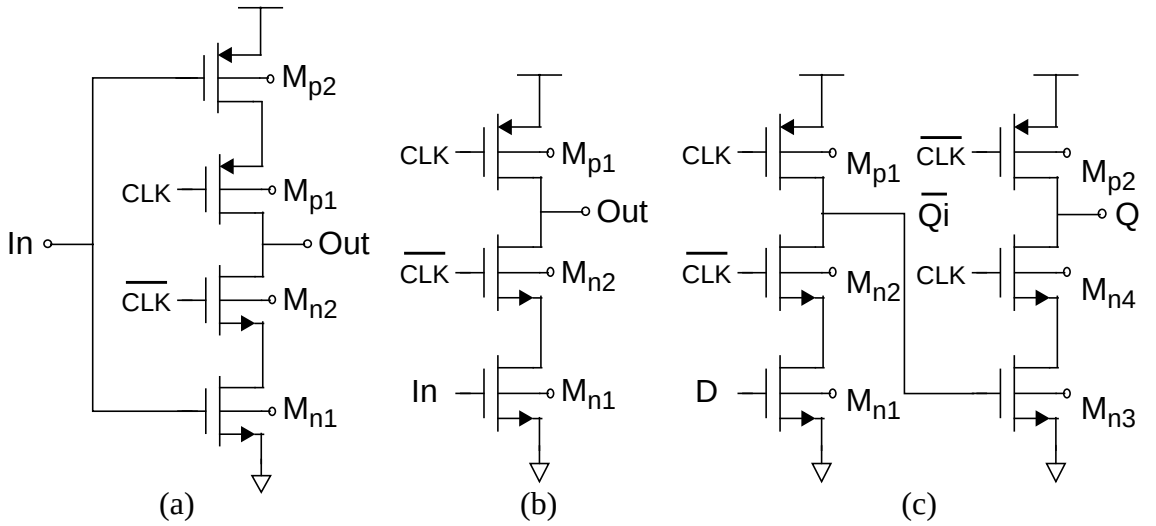


Figure 4-28 Schematics of (a) C^2MOS inverter, (b) $[DP]^2$ inverter or level-sensitive latch and (c) $[DP]^2$ edge-triggered D-Flip-Flop

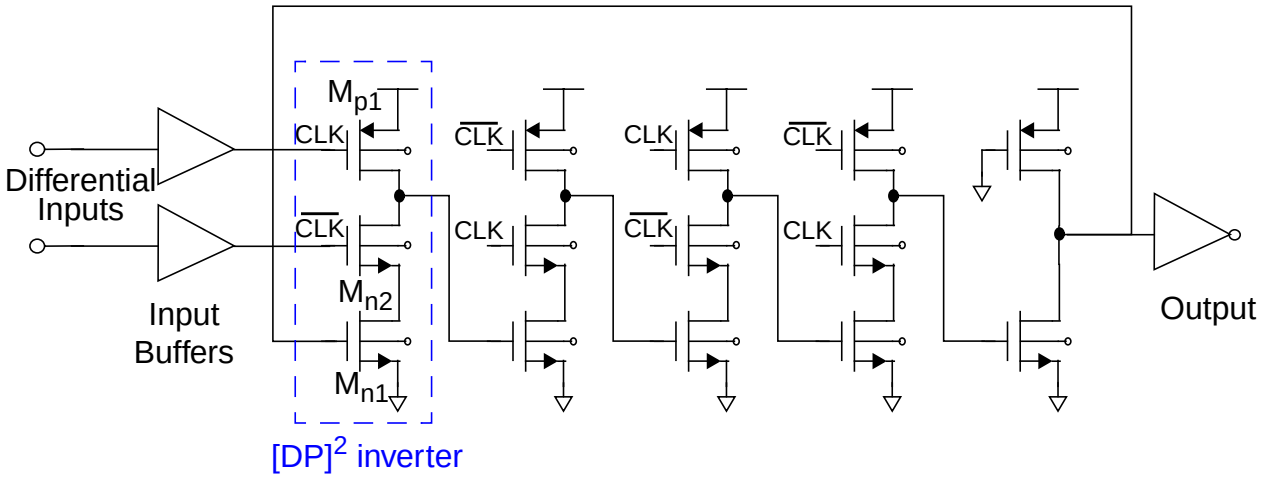


Figure 4-29 Schematic of 4:1 $[DP]^2$ synchronous divider.

period. This delay gives an indication of the speed of standard digital latches used in pipelined circuitry for this process.

Using $[DP]^2$ logic, 4:1 and 128:1 frequency dividers have been implemented [Flo01c] in a partially-scaled 0.1-µm CMOS technology on silicon-on-insulator (SOI) and bulk substrates from IBM. The process uses a 0.35-µm design rule set for all dimensions except for the 0.1-µm gate length and 2.9-nm gate oxide thickness, while providing two metal layers. For SOI, partially-depleted, floating-body transistors are used for all circuitry. A die photograph of the 4:1 divider is shown in Figure 4-30. The die size is 0.51x0.55 mm^2.

4.7.2 Effect of SOI on Circuit Performance

A benefit of using floating body SOI transistors is that the threshold voltage is reduced due to $V_{bs} > 0$. This V_{bs} is caused by charging of the body node through regeneration current [Suh94]. With a lower threshold, the gate-overdrive increases, resulting in more channel current. Hence, the switching speed is increased, resulting in higher maximum operating frequencies for the SOI divider as compared to bulk.

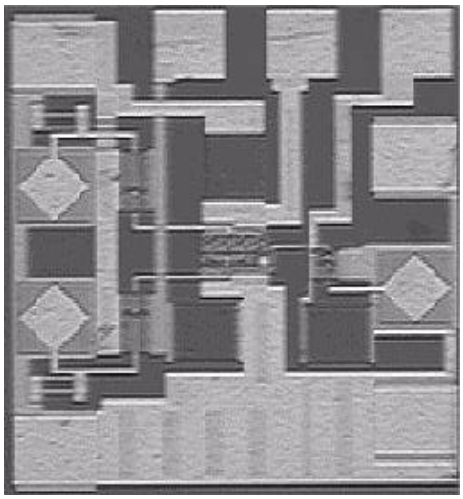


Figure 4-30 Die photograph of 4:1 frequency divider.

The actual maximum operating frequency for the SOI divider is difficult to simulate however, due to the hysteresis of the body voltages. Since the frequency divider will operate continuously, it is important to simulate a steady-state condition for all of the body nodes. The physical mechanism involved in charging V_{bs} at low drain bias is generation current from the drain-body junction [Suh94, Suh95]. This current has to charge what can be modeled as an RC network, with the R defined by recombination current at the source-body junction and the C defined by the capacitance associated with the body, defining a RC time-constant. The combination of a short time-constant at the input switching frequency with a long RC time-constant for the body results in very long computation times to reach a steady state V_{bs}. Therefore, the maximum operating speed of an SOI divider is difficult to simulate due to the amount of time that it takes to reach a steady-state condition for V_{bs} and the number of simulations it takes to scan for the maximum operating frequency.

A final effect of SOI on the $[DP]^2$ divider performance is an increased lower frequency limit due to the presence of a parasitic bipolar device in the transistor. Figure

4-31(a) shows the schematic of a $[DP]^2$ inverter, while Figure 4-31(b) shows the relevant node voltages and device currents simulated using SOISPICE ver4.41 [Fos97]. When in a hold state (CLK=low), a single $[DP]^2$ inverter should retain its previous value at the output node regardless of the input value to the inverter. However when holding a "high" value at the output with a nonzero input, M_{n3} is turned on and its drain is pulled down to ground. This is the situation shown in Figure 4-31(b), where the input is held at ~0.3 V (a low level from pseudo-NMOS) for hold and evaluate. Since the average dynamic V_{bs} of M_{n4} is ~0.8 V and $V_{d,n3}$ is now at ground, a transient bipolar leakage current ($I_{bjt,n4}$) is induced in M_{n4}, despite the input of M_{n4} being held low [Pel95]. This drains the charge stored at the output, causing the inverter to begin to change states when it should be holding. These effects can be seen in Figure 4-31(b), where a BJT current is noticeable, and the output voltage is decreasing. The time constant associated with this bipolar leakage is on the order of nanoseconds for this technology. If the divider is being switched at a rate much

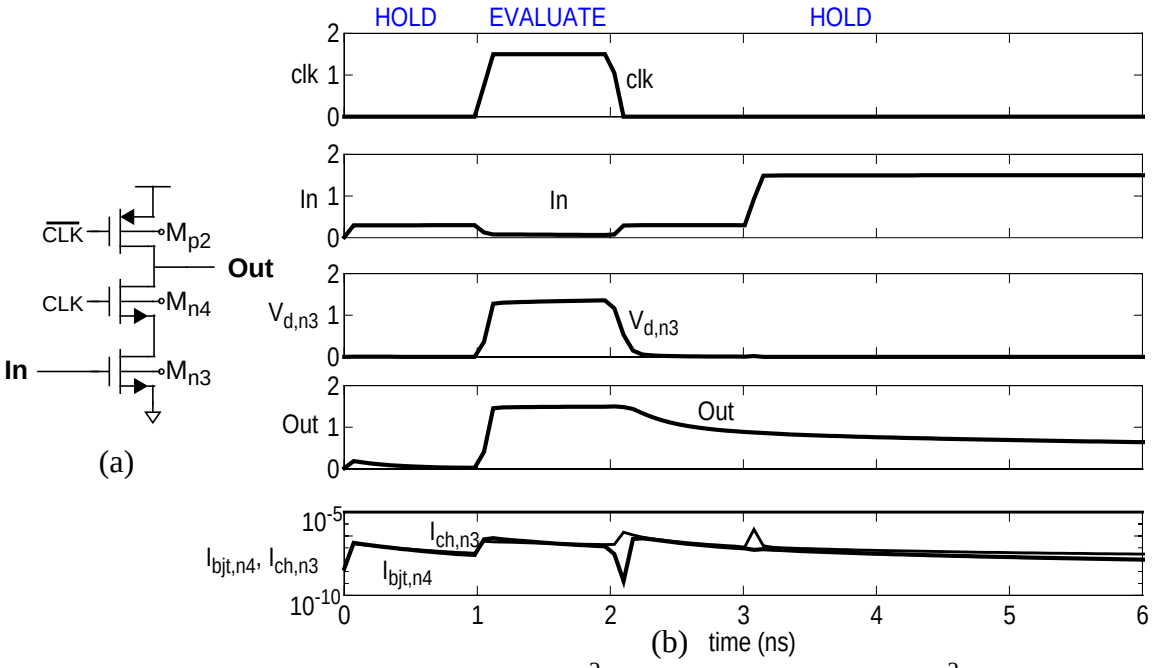


Figure 4-31 Transient bipolar effects of $[DP]^2$ logic. (a) Schematic of $[DP]^2$ inverter and (b) corresponding node voltages and currents.

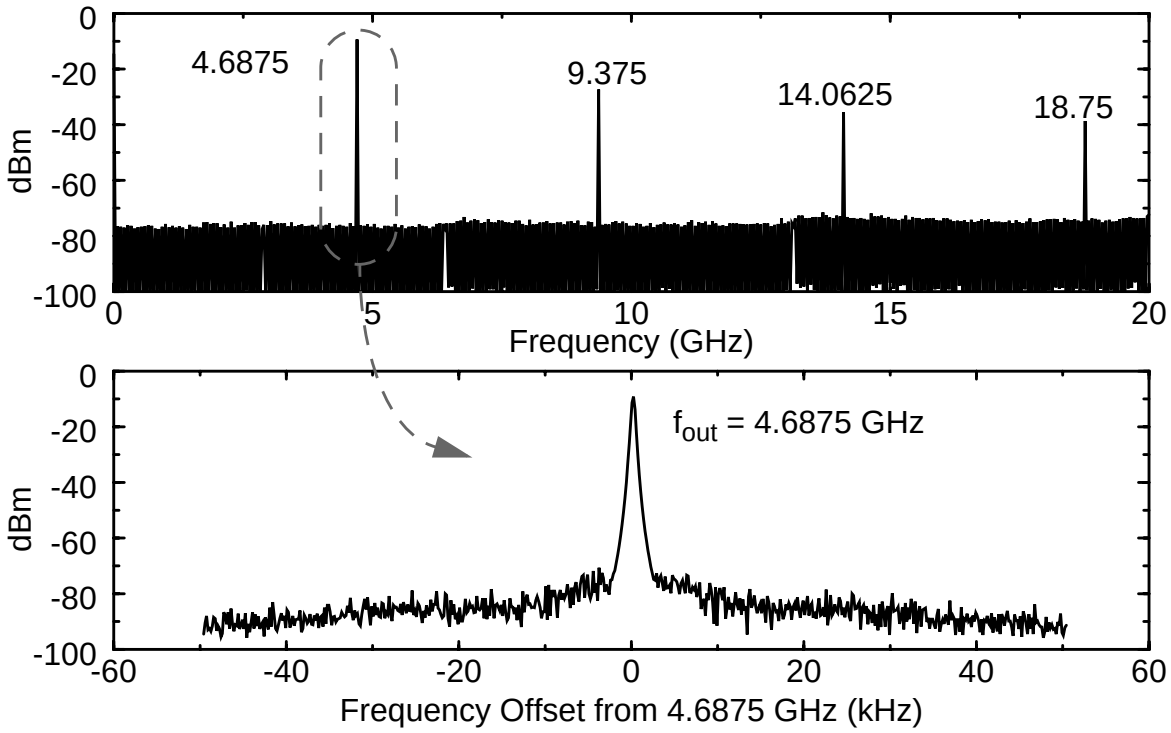


Figure 4-32 Output spectrum of SOI 4:1 frequency divider for f_{in} = 18.75-GHz and V_{dd}=1.5 V.

higher than this, then the bipolar leakage should not degrade performance. However, the lower frequency cutoff for an SOI divider is increased, which can potentially reduce the overall operating frequency range. Another implication of this is that for an SOI $[DP]^2$ divider with a high division-ratio, a different DFF topology is needed for the latter stages.

4.7.3 Measured Results

A 4:1 SOI divider was measured on-wafer using high-frequency probes. A spectrum analyzer was required to examine the output signal due to frequency limitations of the oscilloscope's trigger (trigger frequency limited to 2 GHz). A 180^o coupler was used as a balun to generate the clock and $\overline{clk}$ signals. Measurements show that the SOI divider can operate between frequencies of 9.1 and 18.75 GHz for a 1.5-V supply. Figure 4-32

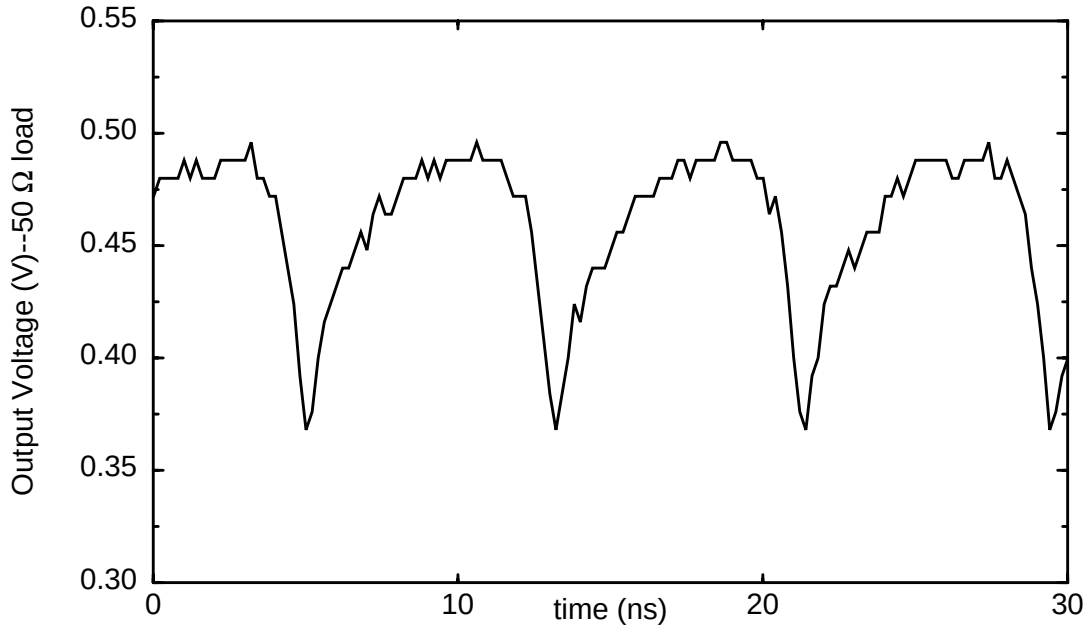


Figure 4-33 Output wave-form for bulk 128:1 frequency divider for 15.36-GHz input signal and V_{dd}=1.5 V. Output frequency is 120 MHz.

shows the output spectrum of the divider for an 18.75-GHz input signal and a 4.6875 GHz output signal. The spectrum also contains higher order harmonics of the output signal. The power consumption of the SOI 4:1 divider is 13.5 mW. From the maximum operating frequency, the extracted SOI $[DP]^2$ level-sensitive latch delay is 13.3 ps at 1.5 V.

A bulk 128:1 divider was also measured on-wafer. This divider consists of the 4:1 $[DP]^2$ divider followed by an asynchronous 32:1 divider implemented with TSPC logic. At 1.5 V, the bulk divider can operate between 3 and 15.4 GHz. As expected, the lower frequency cutoff of the bulk divider is less than that for the SOI divider, due to SOI's transient bipolar leakage. At 15.4 GHz, a 120-MHz output signal is generated, shown in Figure 4-33. The bulk divider power consumption is 9.8 mW. The extracted bulk $[DP]^2$ level-sensitive latch delay is 16.2 ps at 1.5 V. As expected, the bulk latching delay is longer than the SOI latching delay.

Table 4-5 Performance summary for 0.1-µm dividers.

	SOI Divider	Bulk Divider
Division Ratio	4:1	128:1
V_{dd}	1.5 V	1.5 V
Max. Input Freq.	18.75 GHz	15.4 GHz
Output Freq.	4.6875 GHz	120 MHz
Min. Input Freq.	9.1 GHz	< 3.0 GHz
Power (of 4:1 core)	13.5 mW	9.8 mW
$[DP]^2$ latch delay	13.4 ps	16.2 ps

The results are summarized in Table 4-5. This result is the highest operating frequency for a full-swing frequency divider to date. Also, these results show that a 0.1-µm CMOS technology can support digital circuits operating above 15 GHz, and suggest higher operating frequencies for fully-scaled 0.1-µm technology and beyond.

4.8 Summary

An 8:1 divider topology based on a new source-coupled logic latch has been developed. Two different modes of operation have been identified, including a standard digital latching mode and an injection-locked mode. Injection locking is used to synchronize an oscillator to a low-level input signal whose frequency is a superharmonic of the oscillation frequency. Using injection locking allows the divider to lock to very low-level input signals, resulting in conversion gain for the divider.

Using a standard 0.25-µm CMOS process, a 128:1 divider operating up to ~10 GHz for V_{dd} = 2.5 V has been implemented. For this supply voltage, the input-referred self-oscillation frequency is ~7.3 GHz. Thus, the divider can detect very low-level input signals (~40 mV_{pk-pk}) close to this frequency. Using a 0.18-µm CMOS technology with copper interconnects, a 64:1 divider operating up to 15.8 GHz at 1.5 V and 20.4 GHz at

2.1 V has been implemented. Again, this divider can detect very low-level input signals close to the input-referred self oscillation frequency. Both of these results demonstrate that CMOS frequency dividers can operate at the frequency required by the clock receiver and that injection locking can be used to enhance the system gain.

Using the SCL divider topology, a method to offset built-in phase delay differences has been developed. This methodology allows the dividers to be initialized to one of M states, where M represents the division ratio. By doing this, the systematic skew in the system can be reduced to under $\pm\frac{1}{2M}$ percent. Using the 0.18-μm CMOS technology, a divider with this initialization circuity has been implemented. The results show that the circuit is able to initialize to one of 8 different states. However, for a given desired input state, the output will take any of the 8 possible states, rather than the desired state each time. This failure mechanism was identified and a new latch topology has been proposed.

Finally, using a partially-scaled 0.1-μm SOI and bulk CMOS process, a dual-phase dynamic pseudo-NMOS $[DP]^2$ divider has been implemented. These dividers operate up to 18.75 and 15.4 GHz on SOI and bulk substrates, respectively at 1.5 V. This result is the highest known operating frequency to date for a full-swing frequency divider. Also, extracted $[DP]^2$ latch delays are 13.4 and 16.2 ps, respectively, for the SOI and bulk dividers. These results show that 0.1-μm CMOS can support digital circuits operating above 15 GHz, and suggest even higher frequencies for fully-scaled 0.1-μm technology and beyond.

CHAPTER 5
SYSTEM REQUIREMENTS FOR WIRELESS CLOCK DISTRIBUTION

5.1 Overview

Fundamentally, the goals of any interconnect system are to reliably convey a signal from one location to another, to withstand noise and interference, to efficiently use both area and bandwidth (i.e., low cost), and to dissipate minimal power. Not surprisingly, these are the same goals for wireless communications systems. However, while the goals are the same, the terminology and performance metrics used to characterize each type of system are different. Hence, typical interconnect performance metrics have to be converted to metrics for a wireless communications system. In this work, the wireless interconnect system is being utilized for clock distribution; thus, a set of radio-frequency (RF) metrics including gain, noise figure, linearity (IIP3), and matching has to be developed to meet the main clock requirements of skew and jitter.

First, to maximize the power transfer from the clock source to the local clock system, matching, gain, and antenna requirements are discussed. Second, clock skew and jitter are defined. Third, clock skew and jitter are used to set requirements for the power-level at the input of the frequency divider, the signal-to-noise ratio (SNR) at the input of the frequency divider, the noise figure for the LNA with source-follower buffers, and an IIP3 for the LNA and source-follower buffers. Finally, the overall system requirements are summarized and tabulated.

5.2 Power Transfer from Clock Source to Local Clock System

An illustration of the wireless interconnect is shown in Figure 5-1. The wireless interconnect system has to generate a global clock signal (GCLK), broadcast this signal across a distance containing metal interference structures, receive GCLK with the receiving antenna, amplify and divide this down to the local clock signal (LCLK), and then distribute this signal to adjacent circuits. The signal levels in Figure 5-1 are represented as voltage amplitudes in dBV (decibels with respect to 1 V, which is $20\log_{10}\{\text{amplitude}\}$). Voltage should be used at points in the system where the load is capacitive. At points in the system where the impedance is fixed, having a real component, the signal can be expressed in power (i.e., dBm) rather than voltage. The conversion from dBm to dBV depends on the resistance at that point (= R), and is given as follows:

$$dBV = dBm - 10\log_{10}\left(\frac{1000}{2R}\right). \tag{5.1}$$

For a 50-Ω (single-ended) impedance, the conversion is dBV = dBm - 10 dB.

The total gain of the interconnect is the cascaded gains of each component, including any mismatch loss. The output LCLK voltage swing is then the input voltage swing times the total system voltage gain, limited by the supply voltage. Thus, the main things which effect the LCLK swing are as follows: output power of the transmitter, antenna-to-antenna gain including interference effects, total receiver gain, and mismatch loss at the antennas/circuit interface. Each component will be addressed in this section, and nominal values will be recommended.

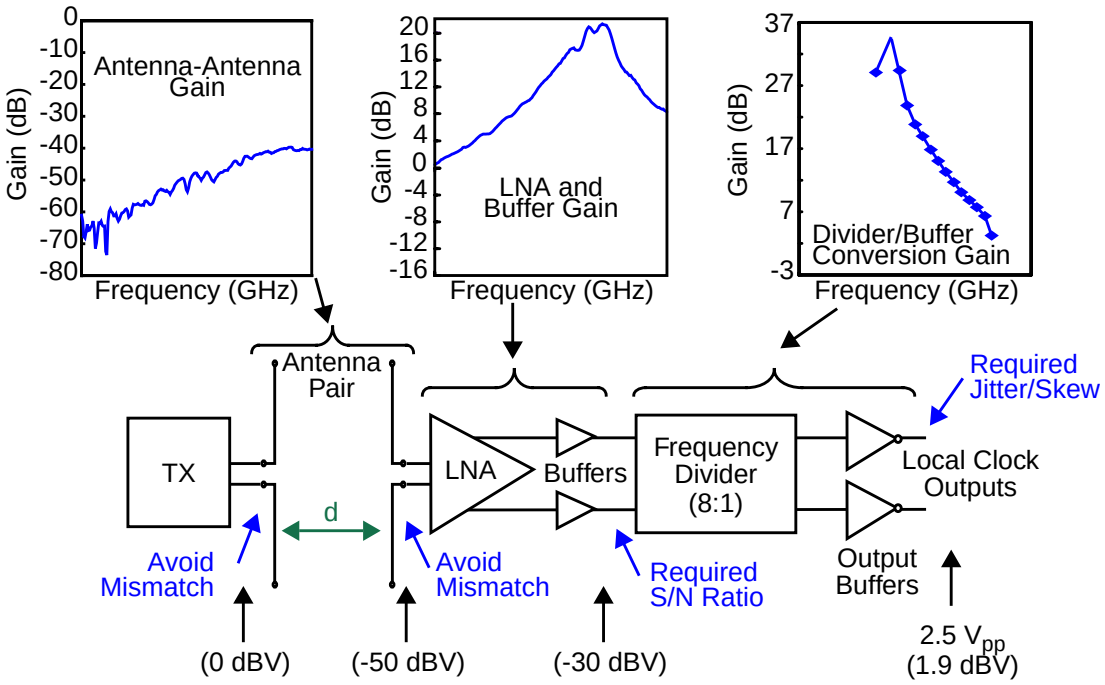


Figure 5-1 Wireless interconnect optimization.

5.2.1 Transmitter Power

The amount of power that the power amplifier (PA) in the transmitter can deliver depends on the supply voltage, the CMOS technology (e.g., gate-oxide thickness), the power amplifier circuit topology, the frequency, and the antenna impedance. Depending on the PA topology (class AB, E, F, etc.), the peak-to-peak voltage swing across the output transistor can be between $2V_{dd}$ and $3.6V_{dd}$ [Lee98]. While recent results have shown CMOS PAs capable of delivering 20-30 dBm of power at 900-1800 MHz using 0.2-0.35-µm technologies [Fal01, Kuo01, Shi01], to the author's knowledge there are no CMOS PA results in the 8 to 20-GHz region other than that which will be presented in chapter 6. Thus, *a 10-dBm output power is set as a goal for the PA at 15 GHz and above*. This corresponds to a peak-to-peak voltage swing of 2 V for a 50-Ω single-ended load. Further work is required to develop CMOS PA's operating above 15 GHz, and the 10-dBm specification should be modified accordingly.

5.2.2 Antenna Specifications

Probably the most critical component for the wireless interconnect system is the antenna. As the loss through the antennas increases, the transmission power and/or the receiver gain have to be increased. Also, any impedance mismatch between the antenna and the circuit (transmitter or receiver) causes reflection or mismatch loss. Finally, the signals will be distributed across a digital chip, which has multiple metal interference and package structures between the antennas. This will further degrade the antenna gain. Due to its importance to the system, the antenna gain and impedance should be accurately predicted for a given antenna structure, distance, and interference pattern. Currently, these predictions have been based on experimental results, however simulation capability is being developed and verified.

Much greater detail on antenna fundamentals and measured antenna characteristics can be found in [Kim00a, Kim00b], as well as in Chapter 6. However, a target antenna gain is needed for subsequent analyses. The 1999 ITRS [SIA99] projects the chip size for a high-performance microprocessor at the 50-nm technology node to be 817 mm^2 (refer to Table 1-1). For a square die with the transmitter at the center and an evenly-spaced grid of 16 clock receivers, the antenna propagation distances will be either 0.5, 1.3, or 1.5 cm. Based on the experimental work presented in [Kim00b], antenna-to-antenna transmission gains of -50 dB and -60 dB are assumed for 1- and 2-cm separation distances at 15 GHz[1], without interference structures. This shows a 10-dB decrease in gain per octave of distance. Using these results, the gains at 0.5, 1.3, and 1.5 cm are extrapolated to be -40, -53,

1. This gain is for a 2-mm long zigzag dipole antenna, 3 μm above a 20-Ω-cm silicon substrate, with a 30^o bend-angle and a 30-μm trace width.

and -56 dB, respectively. Metal interference structures have been shown experimentally (and in Chapter 6) to degrade the gain by 5 to 10 dB [Yoo00, Kim00b]. Applying simple design rules can limit the gain degradation to 7 dB. Thus, *antenna-to-antenna gains of -47 and -63 dB are specified for 0.5- and 1.5-cm distances with interference structures at 15 GHz*. Of course, larger gain at a given frequency will improve the system performance by increasing the signal-to-noise ratio or allowing less power to be transmitted by the power amplifier. Finally, if the loss for a certain distance is too large, preventing system operation, the operating frequency should be increased, since antenna gain increases with frequency. A more advanced technology could be required, though, for the circuits to operate at the higher frequency.

5.2.3 Receiver Gain

A general rule for the receiver is that *the amount of gain in the clock receiver has to approximately equal the amount of loss through the antenna-pair.* Referring to Figure 5-1, the signal at the receiver output is approximately -1.9 dBV, while the signal at the transmitting antenna is ~ 0 dBV. Thus, the gain from the transmitting antenna to the output of the clock receiver is on the order of 0 dB. This is reasonable, since the signals at the input and output of the system should have a peak-to-peak amplitude of ~V_{dd}. Also, this is similar to conventional interconnect systems, where the input and output signals of the interconnect are approximately the same level. The difference is that the wireless interconnect system has considerable loss due to the antennas. Thus, for the nominal antenna gain just specified, the receiver gain should be ~ 63 dB at 15 GHz.

The receiver gain is composed of the LNA and source-follower gain cascaded with the divider conversion gain. Here the utility of using divider conversion gain rather than

input sensitivity is evident. To maximize the receiver gain, *the LNA*[2] *peak gain should occur at a frequency close to the input self-resonant frequency of the divider.* This minimizes the minimum detectable signal of the receiver by allowing for a small-level signal to injection-lock the divider. If needed for testing purposes, the supply voltage of the divider can be adjusted to tune the divider self-resonant frequency. As can be seen, if a divider without conversion gain is used, then either the LNA gain would have to be increased by 20-30 dB, or the transmitter would have to broadcast 20-30 dB more power. Increasing the LNA gain to ~40 dB could lead to circuit instability, while increasing the PA power to >30 dBm is unreasonable. Therefore, dividers with conversion gain are preferable for wireless clock receivers.

5.2.4 Matching Between Antennas and Circuits

To maximize the power transfer from the transmitting antenna to the receiving antenna, the antenna impedance and the impedance of its surrounding circuitry should be conjugately matched. Straying from this conjugate match results in mismatch loss, defined by the following equation [Gon97]:

$$P_{del} = P_{AVS} \cdot M_{ant}, \tag{5.2}$$

where P_{del} is the power delivered from the antenna to the circuit, P_{AVS} is the available power from the antenna, and M_{ant} is the mismatch factor. The mismatch factor is a power transmission coefficient (transmittance) between two mediums. The antenna mismatch factor is given by [Gon97]

2. For the rest of this chapter, when referring to the LNA, both the LNA and source-followers are assumed.

$$M_{ant} = \frac{(1-|\Gamma_c|^2)(1-|\Gamma_{ant}|^2)}{|1-\Gamma_c\Gamma_{ant}|^2}, \tag{5.3}$$

where Γ_c is the reflection coefficient of the circuit and Γ_{ant} is the reflection coefficient of the antenna, both with respect to 100 Ω (differentially). In the wireless clock distribution system, there are two mismatch factors--one at the transmitter and one at the receiver; thus, these factors should be maximized. *The specification for the total mismatch loss (L_{mm}) in the system is 1 dB*, given by the following:

$$L_{mm}|_{dB} = 10\log_{10}\left(\frac{1}{M_{ant1}}\cdot\frac{1}{M_{ant2}}\right). \tag{5.4}$$

Typically, impedance mismatch is specified as either a voltage-standing-wave ratio (VSWR) or a reflection coefficient. These parameters are not straightforward in this system, due to the complex impedances of the source (circuit) and the load (antenna). As was done in [Gon97], equation (5.2) can be rewritten as follows:

$$P_{del} = P_{AVS}\cdot M_{ant} = P_{AVS}\cdot(1-|\Gamma_{eq}|^2), \tag{5.5}$$

where Γ_{eq} is an equivalent reflection coefficient, defined by

$$|\Gamma_{eq}| = \sqrt{1-M_{ant}}. \tag{5.6}$$

Now a VSWR can be defined as

$$VSWR = \frac{1+|\Gamma_{eq}|}{1-|\Gamma_{eq}|}. \tag{5.7}$$

For a 1-dB total mismatch loss, *the equivalent specifications for Γ_{eq} and VSWR at each antenna are -9.6 dB and 2.0, respectively.*

Given an antenna impedance (or reflection coefficient), the range of allowable circuit impedances (or reflection coefficients) is required. Γ_{eq} is expressed in terms of Γ_c and Γ_{ant} by plugging (5.3) into (5.6), resulting in

$$|\Gamma_{eq}| = \left|\frac{\Gamma_c - \Gamma_{ant}^*}{1 - \Gamma_c \Gamma_{ant}}\right|. \quad (5.8)$$

As can be seen, Γ_{eq} is a bilinear transform of Γ_c. A circle with radius $|\Gamma_{eq}|$ (corresponding to M_{ant}, L_{mm}, or VSWR) in the Γ_{eq} plane will, therefore, map into a circle in the Γ_c plane, allowing the circuit impedance to be chosen for a given antenna impedance. Appendix A of [Gon97] contains equations for circle mapping due to bilinear transforms; thus, the derivations are not repeated here. The equation for the circle in the Γ_c plane for a given Γ_{ant} is

$$|\Gamma_c - c| = r, \quad (5.9)$$

where c and r are the center and radius of the circle in the Γ_c plane, given as follows:

$$c = \Gamma_{ant}^* \cdot \left(\frac{1 - |\Gamma_{eq}|^2}{1 - |\Gamma_{eq}|^2 |\Gamma_{ant}|^2}\right) \quad (5.10)$$

$$r = \frac{|\Gamma_{eq}|\left|1 - |\Gamma_{ant}|^2\right|}{1 - |\Gamma_{eq}|^2 |\Gamma_{ant}|^2}. \quad (5.11)$$

As can be seen, for perfect matching (i.e., M=1 or Γ_{eq} = 0), the circle in the Γ_c plane is centered at Γ^*_{ant} with a radius of 0, corresponding to conjugate matching. Figure 5-2 shows a family of circles in the Γ_c plane corresponding to mismatch losses of {-1, -0.5, -0.25, and -0.1} dB, VSWRs of {2.7, 2.0, 1.6, and 1.4}, and Γ_{eq}s of {-6.9 -9.6, -12.5, and -16.4} dB, when reading from the outside circle to the inside circle. These circles are for an antenna impedance of 89-j45 Ω, plotted on a Smith chart normalized by 100 Ω. The second circle from the outside corresponds to VSWR=2; therefore, all circuit impedances located within this circle will meet the system specification, resulting in less than 0.5-dB mismatch loss per antenna.

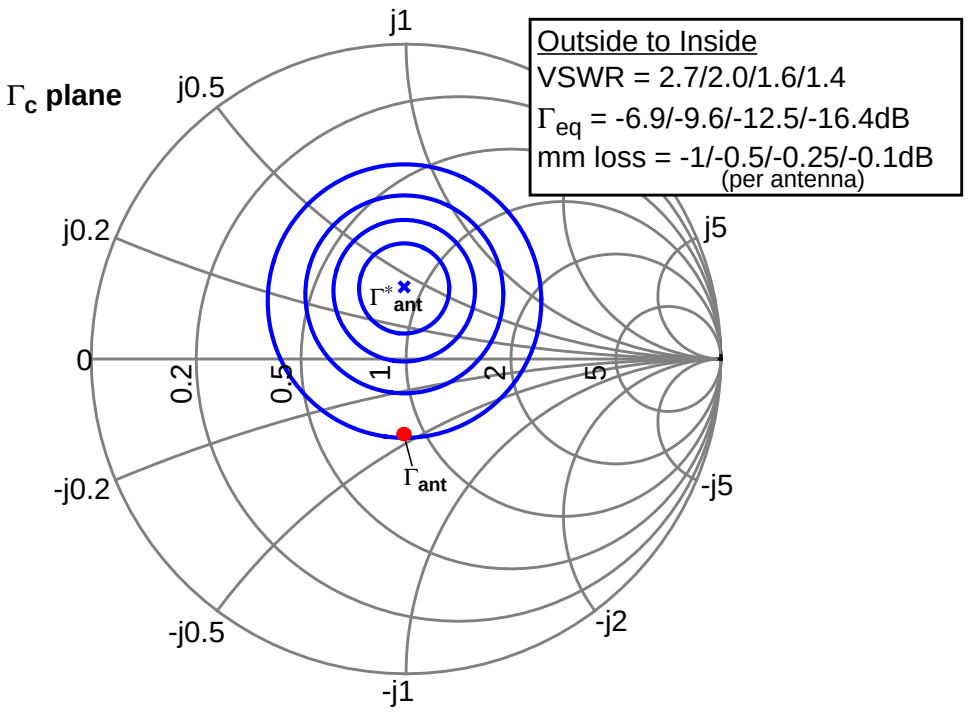


Figure 5-2 Constant Γ_{eq} circles in the Γ_c plane. This shows the allowable circuit impedances for a given antenna reflection coefficient (Γ_{ant} for z_{ant}=(89-j45)/100).

5.3 Definition of Clock Skew and Jitter

A critical requirement for clock distribution systems is ensuring that all of the distributed clock signals are synchronized throughout the chip. Since these clock signals are used to maintain system timing, any uncertainty in the edge of the clock signal reduces the amount of time available to perform useful operations. As a result, the minimum clock cycle time has to be increased by the uncertainty, slowing the system down. Thus, interconnect systems which can deliver high frequency clock signals with minimal timing uncertainty (typically < 5-10% of a clock cycle) are required.

The origin of clock timing uncertainty is mismatch or differences in the propagation delays of the signals. The difference has both time-invariant (static) and time-variant (dynamic) components. *Clock skew* is defined as the static difference between clock edges throughout the chip, while *clock jitter* is defined as the dynamic difference between the

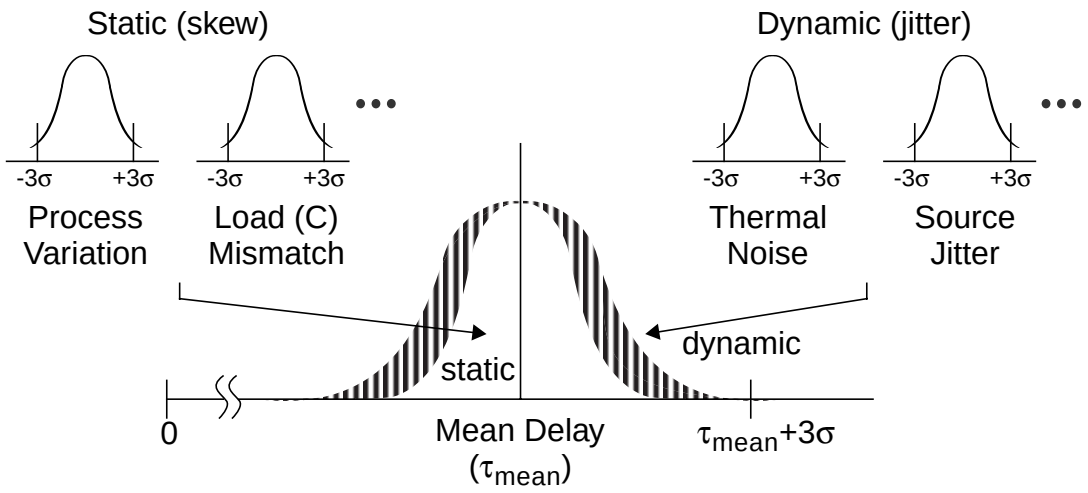


Figure 5-3 Probability density function of propagation delay, including both static and dynamic components resulting in clock skew and jitter (after EDN, July 1995, pp. 35).

clock edges throughout the chip. These quantities are related to the variances (σ^2) of the static and dynamic delay probability density functions (PDF's), respectively.

Figure 5-3 illustrates each type of component as it relates to the total delay PDF. Here, the total static variance is the sum of individual static variances (e.g., process variation, capacitive load mismatch, etc.), yielding the clock skew. Likewise, the total dynamic variance is the sum of individual dynamic variances (e.g., thermal noise, source jitter, etc.), yielding the clock jitter. Both static and dynamic variances add to give the total delay variance. The variances can be quantified as either a peak-to-peak variance (assumed to be ~ 6σ), or a root-mean-squared (RMS) variance (σ), where typically peak-to-peak is used to quantify clock skew and either can be used to quantify clock jitter.

5.4 Clock Skew Versus Amplitude Mismatch

In the wireless clock distribution system, the signals will arrive at the antennas throughout the chip at different power levels, depending on the distance between the

transmitter and receiver. Assuming that the receivers do not correct for this difference in signal strength, then the voltage swing used to trigger or lock the dividers will be much lower in receivers farther from the transmitter. This can potentially lead to a clock skew, due to a conversion from amplitude modulation to phase modulation (AM to FM). The conversion mechanism depends on whether the divider is operating in a latched mode or an injection-locked mode, and each case will be examined.

5.4.1 Latched Mode

For a divider operating in the latched mode, AM-to-FM conversion will result if the divider switches at a point other than the zero-crossing of the input signal. This is illustrated in Figure 5-4. On the left is the case for a divider which triggers at the zero crossing. The output signals for both the high input level and low input level transition at the same time; hence, the divider rejects AM and there is no added clock skew. On the right is the case for a divider which triggers at a point other than the zero crossing, resulting in AM-to-PM conversion or clock skew. The amount of clock skew induced depends on the

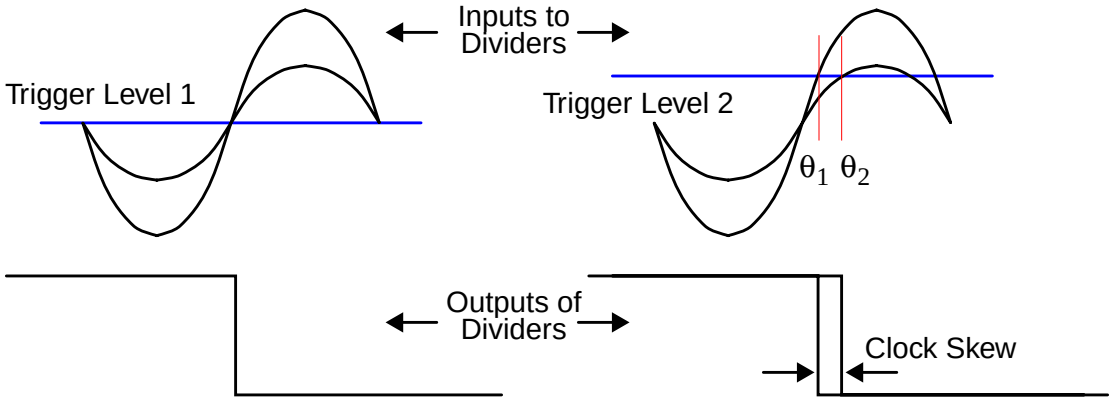


Figure 5-4 Illustrations of AM-to-PM conversion for a divider operating in the latched mode with trigger levels either at the zero crossing (left) or not (right).

trigger level as well as the difference between the low-level and high-level input signals, referred to as amplitude mismatch.

The clock skew as a function of trigger level and input signal levels can readily be obtained. The phase angles, θ_1 and θ_2, at which the maximum and minimum input signals are equal to the trigger level, V_{ref}, are as follows:

$$\theta_1 = \sin^{-1}\left(\frac{V_{ref}}{V_{max}}\right) \tag{5.12}$$

$$\theta_2 = \sin^{-1}\left(\frac{V_{ref}}{V_{min}}\right). \tag{5.13}$$

The clock skew in terms of phase of the input signal is then

$$\Delta\theta_{in} = \sin^{-1}\left(\frac{V_{ref}}{V_{min}}\right) - \sin^{-1}\left(\frac{V_{ref}}{V_{min}} \cdot \frac{V_{min}}{V_{max}}\right). \tag{5.14}$$

Solving for the amplitude mismatch ratio V_{min}/V_{max} yields the allowable signal level difference for a given input angular clock skew, $\Delta\theta_{in}$, as follows:

$$\frac{V_{min}}{V_{max}} = \frac{1}{\delta}[\sin(\sin^{-1}(\delta) - \Delta\theta_{in})], \tag{5.15}$$

where

$$\delta = \frac{V_{ref}}{V_{min}}. \tag{5.16}$$

The maximum clock skew will occur when δ=1. For this case, (5.15) can be reduced to

$$\frac{V_{min}}{V_{max}} = \cos(\Delta\theta_{in}) = \cos\left(2N\pi \cdot \frac{\Delta\tau}{T_{out}}\right), \tag{5.17}$$

where the input angular clock skew has been converted to a clock skew, $\Delta\tau$, with respect to the output local clock period, using the division ratio of the frequency divider, N.

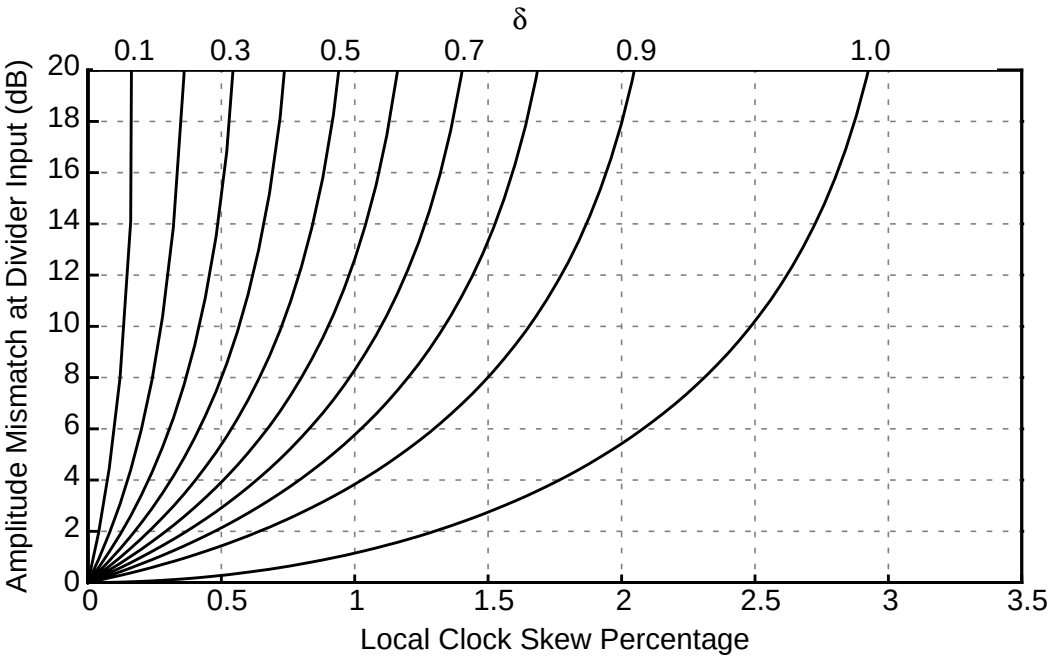


Figure 5-5 Amplitude mismatch allowed at divider input versus local clock skew percentage, with δ varying from 0.1 to 1 in 0.1 increments.

Figure 5-5 shows a plot of the amplitude mismatch in decibels versus local clock skew in percentage, for N=8. These plots are of (5.15) with δ scanning from 0.1 to 1. As δ decreases, a larger amplitude mismatch can be tolerated, meaning that the divider's AM rejection improves as the trigger level approaches zero. As can be seen, for $\delta < 0.3$, the amplitude mismatch can be "infinite" without generating more than ~0.5% of clock skew. The maximum clock skew allowed for amplitude mismatch is set to 0.5%. From (5.17) and Figure 5-5, the amplitudes at the input of the frequency divider should be matched to within 0.3 dB for <0.5% skew, to accommodate the worst-case triggering condition ($\delta=1$).

These results show clock skew as a function of trigger level for different input signal swings to the divider. Dividers utilizing source-coupled logic (SCL) will ideally trigger at the zero crossings of the input signal, due to the differential structure of the SCL D-flip-flop. However, circuit mismatches will cause the trigger level to occur slightly above or below the zero crossings, resulting in a nonzero δ and clock skew. The size of δ

will be small, however, since the offset voltage due to circuit mismatches should be less than 100 mV. In the latched mode, V_{min} is on the order of 0.5-1 V; thus, δ should be less than 0.3, meaning that amplitude mismatch will not cause more than 0.5% of clock skew. As a result, automatic gain control (AGC) should not be required for SCL dividers operating in the latched mode; however, as will be shown, AGC *is* required for dividers operating in the injection-locked mode.

5.4.2 Injection-Locked Mode

When the divider is operating as a superharmonic injection-locked oscillator (ILO), a phase difference exists between the locking signal and oscillator output signal. This phase difference is a function of the input signal levels, as well as the difference between the locking frequency and the natural frequency of the ILO. Appendix E reviews the basic theory behind ILOs. In particular, the steady-state phase relationship between the input and output signals of the ILO was shown to be [Pac65]:

$$\theta_{ss} = \sin^{-1}\left(\frac{\Delta\omega_o A}{\frac{V_L}{V_O}\sqrt{1+(\Delta\omega_o A)^2}}\right) + \sin^{-1}\left(\frac{\Delta\omega_o A}{\sqrt{1+(\Delta\omega_o A)^2}}\right) \qquad (5.18)$$

in equation (E.8). Here, $\Delta\omega_o$ is the difference between the natural and locking frequencies (ω_o-ω_L), A is the derivative of the phase response of the ILO (i.e., 2:1 divider) with respect to frequency ($A = \frac{d\phi}{d\omega}$) from which an equivalent quality factor can be defined, and V_L and V_O are the locking and oscillator output voltage swings, respectively. A phase difference exists because an oscillator generates 360^o of phase-shift around the loop at its natural oscillation frequency. When an input signal is injected into the loop, a phase difference results at that injection point. Therefore, the loop adjusts the oscillation frequency to counteract this phase difference. This is discussed in more detail in Appendix E.

Once again, a clock skew can be defined in terms of the input phase difference in radians. Taking the difference between the steady-state phase difference given in (5.18) for the maximum and minimum input swing locking signals (V_{Lmax}, V_{Lmin}), assuming that the output swings are the same for each case, and making the following substitution

$$\delta_{ILO} = \frac{V_O}{V_{Lmin}} \cdot \frac{\Delta\omega_o A}{\sqrt{1 + (\Delta\omega_o A)^2}}, \tag{5.19}$$

results in (5.15). Thus, the relationship between clock skew and amplitude mismatch at the divider input is the same for dividers operating in the latched or injection-locked mode. In fact, an equivalent trigger level, V_{ref}^{ILO}, can be defined for the ILO divider as follows:

$$V_{ref}^{ILO} = V_O \cdot \frac{\Delta\omega_o A}{\sqrt{1 + (\Delta\omega_o A)^2}}. \tag{5.20}$$

As the locking frequency approaches the natural frequency of the ILO, the equivalent trigger level approaches zero.

The amplitude mismatch for the worst case clock skew can again be quantified. For an injection-locked frequency divider (ILFD), the minimum input signal level will be that for just locking the ILO. This locking condition is given in appendix E in (E.7), where the minimum V_L is

$$V_{Lmin} = V_O \cdot \Delta\omega_o A. \tag{5.21}$$

Plugging this into (5.19), and assuming that $\Delta\omega_o A << 1$ (which is valid in this case since $V_{Lmin} << V_O$), results in $\delta = 1$. With these substitutions, (5.15) becomes

$$\frac{V_{min}}{V_{max}} = 1 \cdot [\sin(\sin^{-1}(1) - \Delta\theta_{in})] = \sin\left(\frac{\pi}{2} - \Delta\theta_{in}\right) = \cos(\Delta\theta_{in}), \tag{5.22}$$

as in (5.17), and Figure 5-5 remains valid. To obtain less than 0.5% of clock skew from amplitude mismatch, the inputs to all of the frequency dividers should be matched to

within 0.3 dB. This worst-case situation occurs when at least one divider is being locked at its minimum detectable signal (MDS). However, in the actual system, the signals at the divider inputs should all be above the MDS, to provide robustness against process variation. Thus, V_{Lmin} increases, and δ decreases. As a result, more amplitude mismatch can be tolerated. If the minimum input signal level at the divider input (V_{Lmin}) is 3 dB above the divider's MDS, then δ would be equal to 0.7, and the amplitude mismatch can be up to 2.9 dB for less than 0.5% of clock skew.

Therefore, AGC is required for dividers operating in the injection-locked mode. This mode, as opposed to the latched mode, will be the most common one for the dividers in the clock receiver, since injection locking increases the conversion gain. The worst-case system specification for the receiver (whose divider is injection-locked) is that *the amplitudes at the input of the frequency divider have to be matched to within 0.3 dB for <0.5% clock skew.* Finally, if the inputs to the dividers are guaranteed to be at least 3 dB above the divider's MDS, then the amplitude mismatch can be as large as 2.9 dB.

5.5 Clock Jitter Versus Signal-to-Noise Ratio

In traditional communications systems, a high signal-to-noise ratio (SNR) is required in order for the receiver to make correct estimations of the modulated data, quantified in terms of a bit-error rate (BER). As the SNR ratio increases, the BER decreases; therefore, a minimum SNR is required such that the BER is lower than that which the modulation code can correct. In the wireless clock distribution system, BER is not really meaningful, since the system is only sending a carrier signal. Instead, noise will corrupt the zero-crossings of the signals, resulting in jitter/phase noise at the output of the frequency divider. Therefore, a relationship between the SNR at the input of the frequency

divider and the output clock jitter is required. To accomplish this, the phase noise of frequency dividers will first be discussed along with the conversion from additive noise to phase noise. Then, the input additive noise to the frequency divider in a clock receiver will be described. Finally, the relationship between phase noise and jitter will be presented and the required SNR for a given jitter will be developed.

5.5.1 Phase Noise of Frequency Dividers

Frequency dividers, by definition, divide the input frequency by the division ratio, N. Since phase is the integral of frequency, dividers reduce the phase by N as well. Phase noise is random variations in the phase of a signal. Therefore, the frequency divider will divide the input phase noise by N^2. For ILFDs, the input phase noise is also filtered by a low-pass response, since the loop will only track phase errors at low frequencies (refer to Appendix E, equation (E.10)). In addition to these, the divider will generate phase noise itself, thus the total output phase noise is the sum of the divided (and filtered, for ILFDs) input phase noise and the added phase noise.

An empirical approach to modeling the phase noise of standard frequency dividers was developed by Egan in [Ega90, Ega91]. He classified the phase noise of a divider as originating from four possible sources. The first source is input phase noise, which is the phase noise of the driving signal on which the divider is operating. The second source is input additive noise, which, when converted to phase noise, will depend on the amplitude of the driving signal (herein lies the dependence on SNR). Both of these components are divided by the division ratio squared when referred to the output. The third source is jitter in the divider, due to variations in the delay it takes a signal to propagate through the circuit. The fourth source is output phase noise which is due to additive noise at the output of

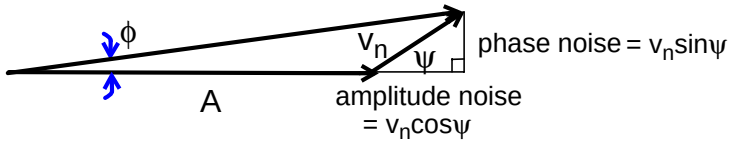


Figure 5-6 Phasor diagram for additive noise, showing how phase noise is generated.

the divider. Since a frequency divider basically samples the input phase during a zero crossing of the signal, the phase noise spectrums will be replicated and aliased at multiples of the sampling frequency [Ega90]. Since there are two zero-crossings per cycle, the sampling rate is twice the output frequency of the divider. The measured results in [Ega90] show that the dominant sources are the output additive noise and the sampled input additive noise. Therefore, these sources will be used to derive the output phase noise as a function of the SNR at the divider input.

5.5.2 Conversion From Additive Noise to Phase Noise

Additive noise, as its name implies, adds to the signals present in the system. This results in both an amplitude and phase fluctuation in the signal. Although this seems straightforward enough, a quick derivation for this case will be presented. In addition, the difference between single-sideband phase-noise density, L, and phase power-spectral-density (PSD), S_ϕ, will be explained to clear up any misconceptions.

Figure 5-6 shows a phasor diagram representing an example where noise is added to a sinusoidal signal with a root-mean-squared (RMS) voltage amplitude, A. The additive noise is represented as $v_n e^{j\psi}$, where v_n is an RMS voltage. This noise can be divided into orthogonal components, where the component parallel to A is defined as amplitude noise, and the component perpendicular to A is defined as phase noise. The phase shift resulting from the additive noise is as follows:

$$\phi = \tan^{-1}\left(\frac{v_n \sin\psi}{A + v_n \cos\psi}\right) \cong \tan^{-1}\left(\frac{v_n \sin\psi}{A}\right) \cong \frac{v_n \sin\psi}{A}, \qquad (5.23)$$

where ϕ is in radians. The first approximation is a result of $v_n << A$, while the second approximation is due to a small-angle assumption. This shows that the amount of phase-shift is approximately equal to the perpendicular component (in volts) divided by the signal level (in volts). Due to the small-angle approximation, the phase noise can either refer to ϕ directly or to the $v_n \sin(\psi)$ component.

The mean squared value of the phase shift is:

$$\overline{\phi^2} = E(\phi^2) = E\left(\frac{v_n^2 \sin^2\psi}{A^2}\right) = \frac{\overline{v_n^2}}{A^2} \cdot \frac{1}{2\pi}\int_0^{2\pi} \sin^2(\psi) d\psi = \frac{\overline{v_n^2}}{2A^2}, \qquad (5.24)$$

where E is the expected-value operator, v_n and ψ are independent, and ψ has a uniform probability density function. The factor of 2 in (5.24) means that half of the additive noise power is in the phase, whereas the other half is in the amplitude. The available power from a resistor is $\overline{v_n^2} = kT \cdot \Delta f$, where k is Boltzmann's constant (1.38 x 10^{-23} J/K) and T is absolute temperature of the system. This PSD is a double-sideband density, meaning that it is for positive frequencies only. Therefore, the conversion from an additive noise source to a phase PSD, $S_\phi(f)$, is

$$S_\phi(f) = \frac{\overline{\phi^2}}{\Delta f} = \frac{\tilde{N}_{add}}{2 \cdot P_{sig} \cdot \Delta f} = \frac{kT}{2 \cdot P_{sig}}, \qquad (5.25)$$

where P_{sig} is the power of the signal (= A_{rms}^2) and $\tilde{N}_{add}$ is the additive noise spectral density. The units of (5.25) are rad^2/Hz.

Phase noise is frequently defined as a single-sideband density, $\mathcal{L}(f)$. Since the phase PSD, $S_\phi(f)$, is a double-sideband density, then $\mathcal{L}(f)$ is simply one half of $S_\phi(f)$ [Ega99], or

$L(f)$ is 3 dB lower than $S_\phi(f)$. Units of dBr/Hz (decibels above 1 rad^2/Hz) are typically used for $S_\phi(f)$ and dBc/Hz (decibels above the power of the carrier) for $L(f)$.

5.5.3 Output Phase Noise of Clock Receiver

Since the frequency divider in the clock receiver is preceded by an LNA (with source-follower buffers), the additive noise spectrum at the input of the divider is

$$\tilde{N}_{divadd} = kT \cdot F(f) \cdot G(f) \cdot \Delta f, \tag{5.26}$$

where F(f) and G(f) are the noise factor and power gain of the LNA. Integrating this PSD over all frequencies yields the total noise power, N_{divT}, as follows:

$$N_{divT} = \int_0^\infty [kT \cdot F(f) \cdot G(f)]df. \tag{5.27}$$

An equivalent noise bandwidth (in Hertz) can be defined as

$$BW_N = \frac{kT \cdot \int_0^\infty F(f)G(f)df}{kT \cdot F(f_o)G(f_o)}, \tag{5.28}$$

where f_o is the resonant frequency of the LNA. The additive PSD in (5.26) is converted to a phase PSD using (5.25) to yield the phase noise at the input of the divider, as follows:

$$S_\phi^{in}(f) = \frac{kT \cdot F(f) \cdot G(f)}{2 \cdot P_{sig}}. \tag{5.29}$$

The phase noise at the output of a divider operating in the latched mode with division ratio N due to the input additive noise is [Ega90]

$$S_\phi^{out}(f) = \frac{kT \cdot F(f) \cdot G(f)}{2N^2 \cdot P_{sig}}. \tag{5.30}$$

When the divider is an ILFD, the noise transfer function from the input to the output is low-pass filtered, like a first-order phase-locked loop, with an equivalent loop bandwidth

of *B* (Hz) given in (E.11). The output phase-noise is then (refer to appendix E)

$$S_{\phi}^{out}(f) = \frac{S_{\phi}^{in}(f)/N^2}{1+\left(\frac{2\pi f}{B}\right)^2}, \tag{5.31}$$

where S_{ϕ}^{in} is given in (5.29). Clearly, the output phase noise of the injection-locked divider is less than that of a divider operating in the latched mode.

As was discussed in 5.5.1, the total output phase noise of the frequency divider will be due to the input additive noise described above, the output additive noise, and the sampling effects of input additive noise. The sampling effects will be accounted for implicitly by integrating the phase noise density over all frequencies which will result in the same total power as the integral of the aliased spectrum from 0 to the sampling frequency. Output additive phase noise will simply add to (5.30).

5.5.4 Jitter in Clock Receiver

As derived in Appendix G and given in [Ega99], the clock jitter at a node is related to the phase noise at that node through the following formula:

$$\sigma_T^2 = \frac{4}{(2\pi f_o)^2} \cdot \int_0^{\infty} S_{\phi}(f)\sin^2(\pi f T)df, \tag{5.32}$$

where T is the observation time. The units of (5.32) are in sec^2. The RMS cycle-to-cycle jitter would be the square root of (5.32) with T equal to the period of the output clock signal. The sine-squared function has nulls at $f = \frac{n}{T}$, or harmonics of the output frequency. If the phase PSD is not varying very fast versus frequency with respect to $\sin^2(\pi fT)$, then the average value of $\sin^2(\pi fT)$ can be used. This results in the following jitter variance:

$$\sigma_T^2 \approx \frac{2}{(2\pi f_o)^2} \cdot \int_0^{\infty} S_{\phi}(f)df \cdot \tag{5.33}$$

Now all the tools are available to derive the relationship between signal-to-noise ratio (SNR) and clock jitter due to input additive noise. The output jitter due to an injection-locked divider will be less than that for a latched divider; hence, (5.30) is used for the output phase noise of the divider, representing the worst case. Plugging (5.30) into (5.33) the total output jitter of the clock receiver due to input additive noise, is as follows:

$$\sigma_T^2 = \frac{2}{(2\pi f_o)^2} \cdot \int_0^\infty \left(\frac{kT \cdot F(f) \cdot G(f)}{2N^2 \cdot P_{sig}} \right) df . \tag{5.34}$$

Substituting (5.27), results in

$$\sigma_T^2 = \frac{1}{(2\pi f_o)^2} \cdot \frac{1}{N^2} \cdot \left(\frac{N_{divT}}{P_{sig}} \right) = \frac{1}{(2\pi f_o)^2} \cdot \frac{1}{N^2} \cdot \left(\frac{1}{SNR} \right). \tag{5.35}$$

The timing jitter can be converted to a phase jitter σ_{cycle} (in cycles or, equivalently, as a percentage of the period) by simply multiplying (5.35) by the frequency squared, yielding

$$\sigma_{cycle}^2 = \frac{1}{(2\pi)^2} \cdot \frac{1}{N^2} \cdot \left(\frac{1}{SNR} \right). \tag{5.36}$$

Figure 5-7 shows a plot of cycle-to-cycle RMS clock jitter versus SNR (in dB) for a division ratio of N=8. As can be seen, as the SNR improves, the clock jitter improves as well. The slope of the line is linear when plotting the jitter on a logarithmic scale, with a slope of 6-dB (SNR) per octave decrease in jitter. To obtain an RMS jitter of 0.5% of the local clock period, a 12-dB SNR is required at the input of the divider. When the SNR is 6 and 0 dB, the local clock jitter is 1% and 2%, respectively. The fact that 0 dB SNR yields only 2% RMS jitter is due to the 8:1 divider reducing the jitter (in percentage) by the division ratio. Thus, the RMS jitter at the input of the divider is 16%. The peak-to-peak jitter at the input of the divider for a 0-dB SNR is then $6\sigma_{in} = 96\%$.

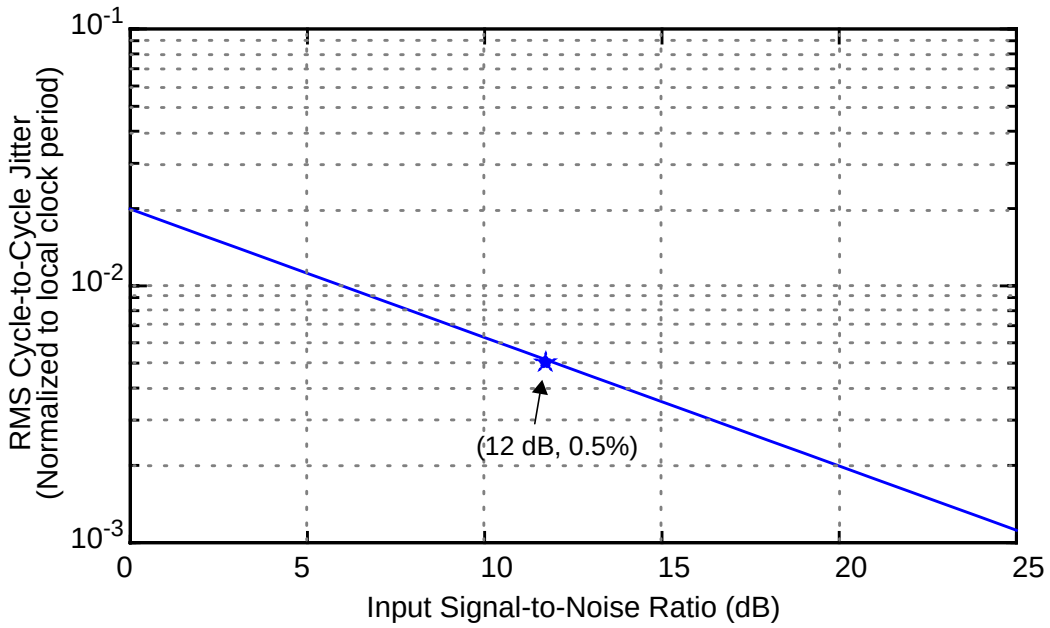


Figure 5-7 Local clock jitter versus signal-to-noise ratio at input to divider.

A survey of jitter results obtained in the literature for high-performance microprocessors [Tam00, Boe99, Kae98, Mai97, You97] reveals that the peak-to-peak cycle-to-cycle jitter should be less than 3% of the clock period, or the RMS cycle-to-cycle jitter should be less than 0.5%. Therefore, *the system specification for the clock receiver is that the SNR at the input of the divider should be at least 12 dB to result in less than 0.5% RMS cycle-to-cycle jitter from input additive noise and interference*.

Finally, as was mentioned earlier, the total phase noise at the output of the divider will have components due to input additive noise and output additive noise. Equation (5.35) calculates the jitter from only input additive noise. Since the output additive noise is independent of input SNR, for high enough SNR's the jitter will no longer decrease. Instead it will level off at some SNR_{knee}, where the jitters from input and output additive noises are equal. As the division ratio increases, SNR_{knee} will decrease. Therefore, the output additive noise sets a floor on the obtainable jitter.

To verify the dependence of jitter on SNR for a frequency divider, a 0.25-μm frequency divider was simulated at 4 different SNRs. To generate transient noise, an array of 30,000 data points randomly distributed according to a gaussian probability density function was generated using Matlab[3]. The mean was set to zero and the standard deviation was set to 1. This array was imported into SPICE at 1-ps time intervals, generating a noise transient voltage 30 ns long. The 1-ps time interval sets the maximum frequency of the noise, while the 30-ns total length of time sets the number of data points which will be obtained from the simulation. In other words, these two numbers basically set the limits of integration for (5.32), with the lower limit set by ~1/(30 ns) and the upper limit set by ~1/(1 ps). By amplifying this noise and adding it in series with the input signal, a given SNR can be obtained. The SNR is simply equal to the ratio of the signal to the standard deviation ($20\log_{10}\left[\frac{V_{sig}}{\sigma}\right]$), and the standard deviation is equal to the amplification factor applied to the noise data. The periods of the 2:1 and 4:1 output signals were then obtained and the standard deviation was calculated. The result is shown in Figure 5-8, which plots the simulated jitter versus SNR, compared with the jitter predicted by (5.35). As can be seen, the simulated jitter for the 2:1 divider agrees very well with the predicted jitter. Clearly, the logarithm of the jitter decreases linearly with SNR (in dB). Also, Figure 5-8 shows that the jitter is decreasing as N becomes larger. Both of these results verify (5.35). However, the simulated jitter for the 4:1 divider is slightly less than the predicted jitter. This is thought to be due to only having half as many data points for the 4:1 periods as compared to the 2:1 periods. Since jitter increases as more data are included

3. This simulation procedure was developed by Jim Caserta, of the University of Florida.

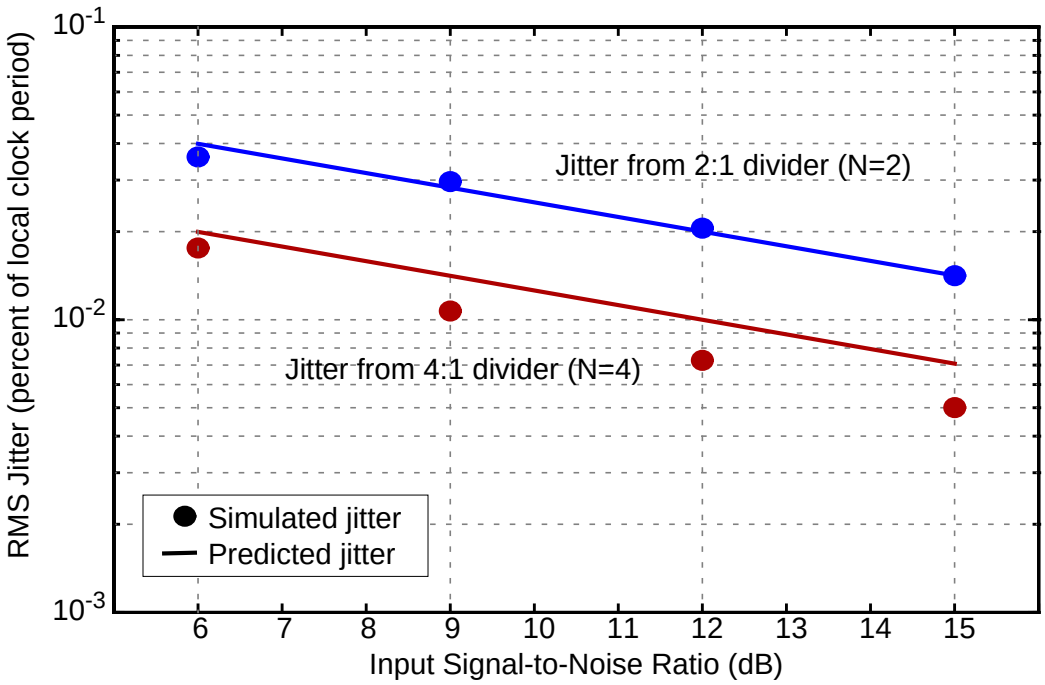


Figure 5-8 Simulation results of RMS jitter versus input SNR from 0.25-µm frequency divider after a division by 2 and division by 4. The simulated jitter (points) is compared to the predicted jitter (line) from (5.35).

(corresponding to integrating the power spectral density to lower frequencies), the difference between the expected and measured jitter is anticipated for short observation times.

5.6 Sensitivity and Noise Requirements

5.6.1 Receiver Sensitivity

Having defined the SNR required at the input of the divider, the receiver sensitivity can now be defined. Sensitivity is defined as the minimum signal level which can be detected for the required SNR. At the divider input, this signal level is

$$P_{sig} = SNR \cdot N_{divT} = SNR \cdot kT \int_0^\infty F(f) \cdot G(f) df \quad , \qquad (5.37)$$
$$= SNR \cdot kT \cdot F(f_o) \cdot G(f_o) \cdot BW_N$$

where (5.27) and (5.28) have been used. The temperature in this equation refers to the equivalent temperature of the antenna, representing the total noise at the input of the

receiver. Note that if the input interference is very large, then the equivalent antenna temperature can be much larger than 298 K [Smi98]. Equivalently, the noise figure can be considered that of the antenna and receiver, where a noise figure for the antenna is defined by the total noise (and interference) at the input of the receiver, divided by the available thermal noise (kT). Note that for very large antenna noise figures, the noise figure of the receiver becomes unimportant, meaning that the noise added by the receiver is a small fraction of the noise already present at the input.

Converting (5.37) to dB and dBm yields the following for T = 353 K (80^{o} C, which is assumed to be the temperature of the microprocessor):

$$P_{sig}\big|_{dBm} = -173\,\frac{dBm}{Hz} + NF(f_o) + G(f_o)\big|_{dB} + 10\log_{10}(BW_N) + SNR_{min}\big|_{dB}. \quad (5.38)$$

Subtracting the LNA gain ($G(f_o)|_{dB}$) from the signal power at the divider input and substituting SNR_{min} = 12 dB, yields the input sensitivity for the clock receiver, as follows:

$$P_{sens}\big|_{dBm} = -161\,\frac{dBm}{Hz} + NF(f_o) + 10\log_{10}(BW_N). \quad (5.39)$$

Referring back to section 5.2, the transmitter power level is specified to be 10 dBm, the antenna-to-antenna gain is specified to be -63 dB at a 1.5-cm distance, and the mismatch loss is specified to be 1 dB. *Therefore, the desired sensitivity is -54 dBm* (10 dBm - 63 dB - 1 dB = -54).

5.6.2 Receiver Noise Requirements

The noise performance of the receiver can now be specified by plugging in the -54-dBm sensitivity into (5.39). This yields the noise figure of the receiver at the center frequency and the noise bandwidth, as follows:

$$NF(f_o) + 10\log_{10}(BW_N) \le 107dB. \tag{5.40}$$

The difficulty with this equation is that BW_N is defined through simulations. As defined, BW_N is the bandwidth from which most of the thermal noise is generated. Since the LNA is a tuned circuit, both the input thermal noise and most of the noise generated in the LNA will be shaped by the tuned response. The response of the LNA can be modeled by the response of a parallel RLC network driven by a current source. Simulations show that the BW_N for a parallel RLC network with quality factor, Q_{Ld}, and resonant frequency, f_o, is

$$BW_N \approx 2\frac{f_o}{Q_{Ld}}. \tag{5.41}$$

Referring to the results in Chapter 3, Q_{Ld} is approximately 10 at 10 GHz (for the 0.25-µm LNA) and 15 at 15 GHz for the 0.18-µm LNA. Thus, $BW_N \cong 2$ GHz and $10\log_{10}(BW_N) = 93$ dB. With this assumption, the maximum noise figure can be specified as 14 dB, with the explicit equation being

$$NF(f_o)_{max} = P_{sens}\big|_{dBm} - 10\log\left(\frac{kT_{eq}}{0.001}\right) - SNR_{min}\big|_{dB} - 10\log_{10}(BW_N). \tag{5.42}$$

Thus, *the system specification for maximum noise figure of the receiver, including the antenna noise figure, at f_o is set to 14 dB.*

This noise figure specification is for a -54-dBm sensitivity. However, as mentioned earlier, if the input interference to the antenna is significant, then the NF in (5.42) is the total noise figure of the antenna plus the receiver (i.e., $F_{ant} + F_{rcvr} - 1$). As the total noise and interference at the receiver input is quantified, the 14-dB specification for NF may become infeasible. As such, the sensitivity of the receiver will have to be modified to a larger power to maintain the 12-dB SNR at the divider input. In other words, currently, the sensitivity specification is driving the noise figure specification. However, with the total

noise and interference at the input of the receiver fully quantified, this noise will drive the sensitivity specification.

5.7 Estimation of Total Noise, SNR, and Jitter for 0.25-µm Receiver

The concepts in the past two sections have been applied to the 0.25-µm LNA and source-follower circuits. Figure 5-9(a) shows the simulated gain and NF for the LNA. The maximum gain is 22.8 dB and the minimum NF is 6.4 dB at 8 GHz. Figure 5-9(b) shows the power spectral density of the noise at the input of the frequency divider, which was given in (5.26). Integrating this PSD over all frequencies yields the total thermal noise power--N_{divT} from (5.27)--which is -53 dBm. To perform an integral in SPICE over all frequencies, the frequency limits are increased until the total integral does not change (~40 GHz for this case). Using the values 22.8 and 6.4 dB for $G(f_o)$ and $NF(f_o)$, respectively, and N_{divT} of -53 dBm, BW_N is calculated to be 1.5 GHz. This is shown in Figure 5-9(b),

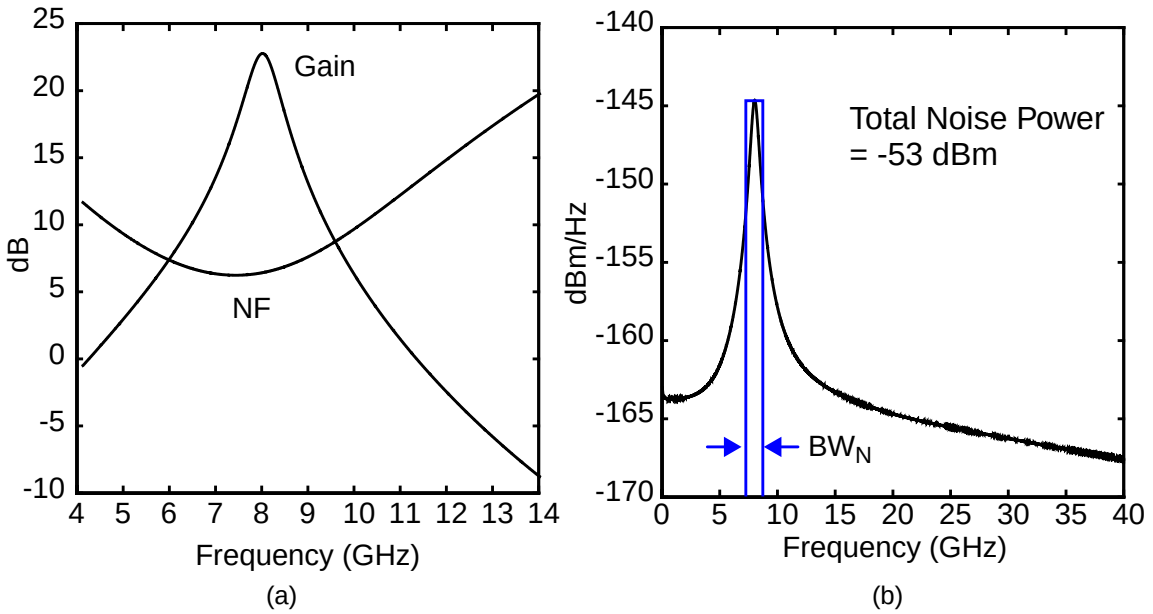


Figure 5-9 (a) Simulated gain and noise figure for 0.25-µm LNA with source-followers. (b) Simulated power spectral density of thermal noise at input of frequency divider, along with equivalent noise bandwidth (BW_N).

where the PSD is fixed at the center-frequency value across the noise bandwidth. The noise bandwidth agrees very well with the estimated value of 2 GHz given in (5.41).

The SNR can now be calculated assuming that the input signal to the receiver is -54 dBm, and that the total input noise is dominated by thermal noise (as was similarly done in [Brav00b]). The -54-dBm input power is the desired sensitivity, which again is a result of 10-dBm transmitted power, -56-dB antenna-to-antenna gain at 1.5 cm, 7 dB of interference effects, and 1 dB of mismatch loss. The signal power level at the input of the divider is -54 dBm plus the gain of the LNA (22.8 dB), or -31.2 dBm. Therefore, the simulated SNR is -31.2 dBm - (-53 dBm) = 21.8 dB. Applying the 21.8-dB SNR to (5.35), the expected RMS cycle-to-cycle jitter is 1.6 ps at the output clock frequency of 1 GHz, corresponding to 0.16% RMS jitter. The peak-to-peak jitter is 9.7 ps, which is ~1% of the clock period. This easily meets the specification of less than 3% of peak-to-peak jitter.

5.8 Linearity Specification

Nonlinearity in the LNA (with source-followers) will result in the following main effects: generation of harmonics, gain compression specified in terms of a 1-dB compression point (P_{1dB}), and intermodulation specified in terms of a third-order intercept point (IP3). A difficulty encountered in the clock receiver is the fact that the signals outside of the “band of interest” are not heavily attenuated. In other words, the response of the LNA is very broadband due to the limited inductor Q in the LNA. Therefore, interfering signals themselves pose more of a problem than the harmonics or intermodulation products these signals generate. In fact, if the interfering signals become too large, they can lock the divider at a different frequency, even with the reduced gain of the LNA at the interferer’s frequency. At the very least, these interfering signals will degrade the SNR, increasing the

clock jitter. Though not the main concern, the harmonics and intermodulation products will still degrade the SNR.

One of the main reasons the global clock is distributed at a higher frequency than the local clock is to try to operate in a band which is not as noisy. The system will be generating a significant amount of noise at and below the local clock frequency, and at frequencies due to the edge-rates of the signals. One potential problematic frequency is around one-third of the global clock frequency[4] (GCLK). Due to nonlinearity, the LNA will generate a harmonic near GCLK. When this signal is added to the desired global clock, the SNR will decrease and jitter will increase. This scenario can then be used to specify the IIP3 of the LNA. Note that a scenario exists for the case of two interferers generating an intermodulation product. However, since these interferers must be far enough away from GCLK to prevent divider locking, the IIP3 would be very similar to the case discussed here.

Figure 5-10 shows an illustration of the case being considered. Two sinusoidal input signals are present at the input of the receiver. One is at the global clock frequency (f_o) having a voltage amplitude, A_{sens}, corresponding to the sensitivity. The interfering signal is at a frequency, $\frac{f_o}{3}$, with an amplitude, A_{int}. The response of a nonlinear LNA can be modeled with a power series as

$$y(t) = \alpha_1 \cdot x(t) + \alpha_2 \cdot x^2(t) + \alpha_3 \cdot x^3(t) + \ldots, \tag{5.43}$$

4. For the wireless clock distribution system, the local clock frequency will be at 1/8 of GCLK. Assuming that this local clock signal is square, its third harmonic will be quite strong, occurring at a frequency of 3/8 (or 0.375) of the GCLK. This subsequently can generate a third-order harmonic at 9/8 (or 1.125) of the GCLK due to LNA nonlinearities.

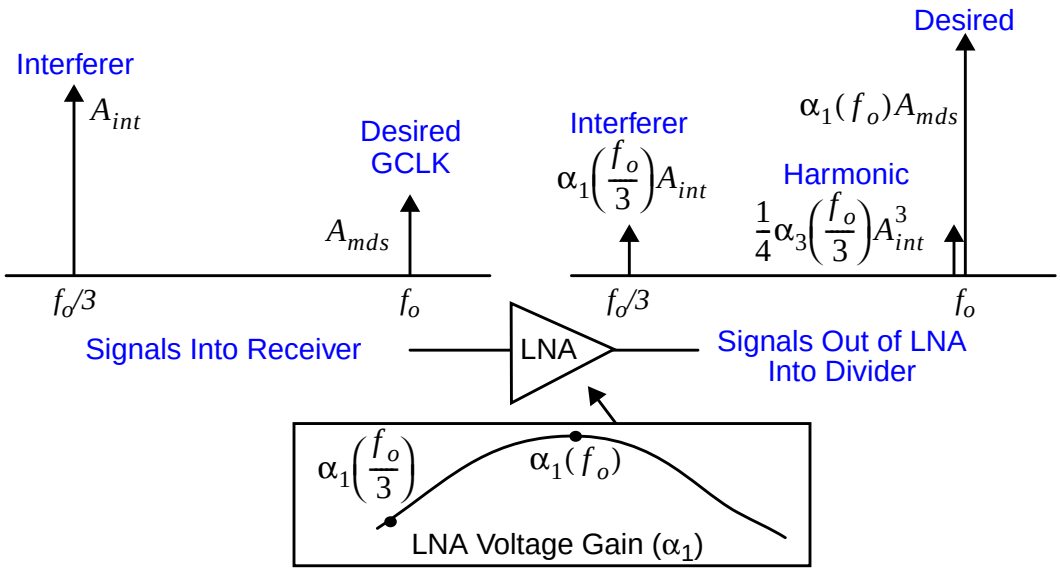


Figure 5-10 Illustration of scenario used to specify LNA IIP3.

where x and y are the input and output of the LNA, α_1 is the gain of the LNA, and α_2 and α_3 are the second- and third-order nonlinearity voltage coefficients, respectively. For a fully-differential circuit, the even-order nonlinearity coefficients are close to zero [Raz95]. Therefore, the output from the LNA for the interfering signal at $\frac{f_o}{3}$ is as follows:

$$y(t) = \left[\alpha_1\left(\frac{f_o}{3}\right)A_{int} + \frac{3}{4}\alpha_3\left(\frac{f_o}{3}\right)A_{int}^3\right]\cos\left(2\pi\frac{f_o}{3}t\right) + \frac{1}{4}\alpha_3\left(\frac{f_o}{3}\right)A_{int}^3\cos(2\pi f_o t), \quad (5.44)$$

where the frequency dependence of the α parameters has been included. The third-harmonic term in this expression will interfere with the desired GCLK signal, degrading the SNR and eventually overtaking the desired signal.

The scenario used to specify IIP3 is now described. Integral to any IIP3 specification is the constraint on the power of the interferer. In the case of the clock receiver, the power of the interferer is constrained by setting the ratio between the output power of the desired signal at f_o, when it is at its sensitivity, to the output power of the interferer at $\frac{f_o}{3}$ to the required SNR to meet a given jitter specification. In equation form, this is written as

$$\frac{[\alpha_1(f_o)A_{sens}]^2}{[\alpha_1(f_o/3)A_{int}]^2} = SNR(\sigma_T), \tag{5.45}$$

where SNR(σ_T) is given in (5.35). Nonlinearity will generate a third-order harmonic of the interferer, which will corrupt the SNR. The IIP3 is specified for the case when the SNR is degraded by 3 dB due to this third-order harmonic. Thus, the output power of the third-order harmonic at f_o should be equal to the output power of the interferer at $\frac{f_o}{3}$. This results in

$$\left[\alpha_1\left(\frac{f_o}{3}\right)A_{int}\right]^2 = \left[\frac{1}{4}\alpha_3\left(\frac{f_o}{3}\right)A_{int}^3\right]^2. \tag{5.46}$$

The ratio of α_1 to α_3 can be related to the IIP3 at that frequency [Raz95]. Since $\alpha_3\left(\frac{f_o}{3}\right)$ is not a readily-known quantity the following assumption is made:

$$\frac{\alpha_1(f_o)}{\alpha_3(f_o)} = \frac{\alpha_1\left(\frac{f_o}{3}\right)}{\alpha_3\left(\frac{f_o}{3}\right)} = \frac{3}{4}A_{IIP3}^2. \tag{5.47}$$

This assumption states that the third-order nonlinearity has the same frequency response as the gain, or equivalently, that IIP3(f_o) is equal to IIP3($\frac{f_o}{3}$).

Using (5.45) and (5.47) in (5.46) results in the following expression for A_{IIP3} (the input amplitude in Volts corresponding to IIP3 in Watts):

$$A_{IIP3} = \frac{\sqrt{3}}{3}\cdot\frac{\alpha_1(f_o)}{\alpha_1\left(\frac{f_o}{3}\right)}\cdot\frac{A_{sens}}{\sqrt{SNR(\sigma_T)}}. \tag{5.48}$$

This can be expressed in dBm as follows:

$$IIP3\big|_{dBm} = P_{sens}\big|_{dBm} + G_{LNA}(f_o)\big|_{dB} - G_{LNA}\left(\frac{f_o}{3}\right)\Big|_{dB} - SNR(\sigma_T)\big|_{dB} - 4.8 \tag{5.49}$$

The LNA gain at $f_o/3$ can be found from simulations. These simulations show that the *attenuation* at $f_o/3$ is approximately 10 dB less than the gain at f_o. If half of the gain in the receiver is the gain in the LNA, then for a -54-dBm sensitivity, a 63-dB receiver gain, and a 6-dB SNR (for 1% RMS jitter), the specified IIP3 is -54 + 31.5 - (-21.5) - 6 - 4.8 = -11.8 dBm. Although this 1% RMS jitter is more than the 0.5% target, this results in a more aggressive IIP3 specification. *Thus, the system specification for IIP3 is -12 dBm.*

5.9 Summary

In this chapter, system specifications have been developed for a wireless clock distribution system, converting standard clock metrics into RF metrics. To maximize the power transfer from the clock source to the local clock system, matching, gain, and antenna requirements have been specified. In particular, the receiver gain should approximately equal the loss through the antennas. Clock skew and jitter have been defined and are used to set the remaining performance metrics of the system. Amplitude mismatch at the input of the frequency divider results in clock skew, thus the signal-levels at the input of the divider should be equal. Thermal noise at the input of the divider will result in clock jitter, due to its conversion to phase noise. As the signal-to-noise ratio (SNR) improves, the jitter decreases, and a minimum SNR at the input of the frequency divider is specified. A 6-dB increase in the SNR halves the clock jitter. Using the SNR, a receiver sensitivity is specified, the total output noise from the LNA with source-follower buffers is determined, a noise figure is specified, and an IIP3 for the LNA and source-follower buffers is derived.

Table 5-1 summarizes the system specifications. These specifications are listed for a 15-GHz global clock frequency, where the following are dependent on this frequency: antenna-to-antenna gain, receiver gain, receiver sensitivity, noise figure, and IIP3. If a

different global clock frequency is to be used, then these specifications can be modified using the formulas presented in this chapter.

Some general requirements for the system which have not been discussed include power consumption, balanced topology, and passive components. First, the power consumption is specified to be 40 mW per receiver at 1.5 V_{dd}. This number is based on the analyses performed in Chapter 7, resulting in the power consumption of the wireless clock distribution being comparable to that of conventional grid and H-tree distribution systems. Second, the receiver should employ a balanced topology. This will obviate the need for a balanced-to-unbalanced conversion between the antenna and LNA, reject common-mode noise [Meh98, Brav00a], and provide dual-phase clock signals to the frequency divider. Common-mode noise rejection will reduce the interference picked up by the receiver; hence the SNR will improve and the jitter will decrease. Finally, the quality factors of the passive components should be large. In silicon integrated circuits, typically the inductor Q will limit the performance of the system. This is the case with CMOS LNAs, as shown in Chapters 2 and 3. This will be further exemplified in Chapter 6 in the presentation of the 0.18-μm clock transmitter and receiver results. As the inductor Q improves, the equivalent noise bandwidth will decrease, noise figure will decrease, receiver gain will increase, SNR will increase, and clock jitter will decrease. Clearly, Q is integral to the performance of the entire system. Based on the results presented in Chapter 6, inductor Q's of ~30 at 15 GHz are recommended. However, as has been shown in Chapter 2 and will be shown in Chapter 7, high-Q circuits are more susceptible to process variations; thus, there are trade-offs involved in choosing the inductor Q. More work is required to develop the optimal Q and/or to develop high-Q circuits which are not as susceptible to process variations.

Table 5-1 System specifications for wireless clock distribution at 15 GHz.

Performance Metric	Specification
Global clock frequency	15 GHz
Local Clock Frequency	1.875 GHz
Output Clock Skew	< 5% (of local clock period)
Output Clock Jitter	Peak-to-peak cycle-to-cycle < 3% RMS cycle-to-cycle < 0.5%
Transmitter Power	10 dBm
Antenna-to-Antenna Gain with Interference^{+}	-47 dB at 0.5-cm separation -63 dB at 1.5-cm separation (both including 7-dB interference loss)
Receiver Gain^{+}	63 dB (Gain ≅ antenna-pair loss) (LNA resonant freq. = f_{iSO} of divider)
Matching Between Antenna and Circuit	Total mismatch loss < 1 dB; Γ_{eq} < -9.6 dB; VSWR < 2.0
Receiver Sensitivity^{+}	-54 dBm
Noise Figure^{+}	14 dB
IIP3^{+}	-12 dBm
Amplitude Matching at Divider Input (for <0.5% clock skew)	within 0.3 dB (worst-case: at least 1 divider at MDS) within 2.9 dB (all dividers at least > MDS + 3 dB)
Signal-to-Noise Ratio at Divider Input	12 dB (for < 0.5% RMS jitter)
Receiver Power Consumption	40 mW per receiver at 1.5 V_{dd}

$^{+}$Note: These specifications are dependent on global clock frequency.

CHAPTER 6
WIRELESS INTERCONNECTS FOR CLOCK DISTRIBUTION

6.1 Overview

The clock receiver, shown in Figure 1-3(b), contains an integrated receiving antenna, a fully-differential LNA, a pair of source-follower buffers, a frequency divider which translates the global clock frequency to the local clock frequency, and output buffers which drive the local-clock capacitive load. The design and implementation of CMOS LNAs and frequency dividers has been presented in chapters 2-4, while chapter 5 presented the system requirements for wireless clock distribution. This chapter uses these concepts and circuits to implement wireless interconnect systems and to demonstrate system operation. A critical component of a wireless interconnect system is the antenna, which acts as a transducer between the electromagnetic wave and the current and voltage within the circuitry. This chapter presents a brief review of antenna fundamentals. Then, the measured characteristics of on-chip antenna pairs and antennas connected to an LNA are presented. These results are from a 0.25-μm CMOS test chip. Using this chip, a 7.4-GHz single-receiver wireless interconnect across a 3.3-mm distance is presented--the first on-chip CMOS wireless interconnect ever demonstrated. A second test chip was implemented in a 0.18-μm CMOS process with copper interconnects. In this chip, multiple antenna test structures are included and characterized. Also, in the 0.18-μm test chip, single-receiver and double-receiver wireless interconnects are demonstrated across 5.6- and 6.8-mm interconnection distances at 15 GHz. These receivers have initialization

circuitry to reduce the clock skew. Finally, a wireless clock transmitter (not in a PLL) has been implemented, characterized, and demonstrated for a 5.6-mm interconnection distance. These results conclusively demonstrate system operation and plausibility.

6.2 On-Chip Antennas

6.2.1 Antenna Fundamentals

To evaluate on-chip antennas, a review of basic antenna fundamentals is required, such as radiation resistance, antenna impedance, directivity, antenna gain, and near/far-field definitions. *Radiation resistance* (R_r) is equal to the total power radiated by the antenna divided by the root-mean-squared (rms) current in the antenna. Hence, R_r represents the radiation of an antenna. An antenna with a small radiation resistance indicates that a large current would be required to radiate power. Keep in mind that antennas are reciprocal, which means that the radiation properties apply both to an antenna's transmitting and receiving capabilities.

The *antenna impedance* is the impedance "seen" looking into the antenna, defined as the ratio of voltage to current at the antenna terminals. The antenna resistance is composed of the radiation resistance and loss resistance of the antenna, as well as substrate components. The antenna reactance is composed of the capacitance and inductance of the antenna lines as well as the substrate components. To maximize the power transfer between the antenna and the circuitry, the circuit impedance should be the conjugate of the antenna impedance.

Directivity (D) is a figure-of-merit used to quantify the directional properties of an antenna. The directivity of an antenna is the radiation intensity (radiated power per unit solid angle) for that antenna in a given direction divided by the radiation intensity of a

non-directive or isotropic antenna. Hence, the directivity is maximum in the direction of maximum radiation. The higher the directivity, the stronger the antenna's radiated energy is for that direction. All practical antennas are directional (D>1), in that the directivity is not constant for all directions. A subcategory of directional antennas is the omnidirectional antenna, whose directivity is essentially constant across a certain plane.

The gain between a transmitting/receiving antenna pair can be determined using Friis transmission equation [Bal97], which describes the power received to the power transmitted between two antennas as follows:

$$\frac{P_r}{P_t} = e_t e_r \cdot (1 - |\Gamma_t|^2)(1 - |\Gamma_r|^2) D_t D_r \left(\frac{\lambda}{4\pi r}\right)^2, \qquad (6.1)$$

where e_i is an efficiency representing loss in the conductors and dielectrics (equal to the radiation resistance divided by the sum of the radiation resistance and the loss resistance [Bal97]), Γ_i is the reflection coefficient at the antenna terminals, D_i is the directivity, and λ and r are the wavelength and separation distance, respectively. When characterizing an antenna pair using S-parameters, this Friis transmission equation is equal to $|S_{21}|^2$ [Kim00a], which is equal to the *transducer gain* (G_T), when the antennas are measured with 50-Ω transmission lines and termination impedances [Gon97]. To characterize the antenna performance under matched conditions, a *transmission gain* (G_a) is defined as

$$G_a = \frac{|S_{21}|^2}{(1 - |S_{11}|^2)(1 - |S_{22}|^2)}. \qquad (6.2)$$

Referring to (6.1), G_a is equal to the quantity $e_t e_r D_t D_r (\lambda/4\pi r)^2$. This gain is equal to the power available at the output divided by the power delivered to the input, representing the best possible gain for the antennas, where both antennas are conjugately matched.

Therefore, G_a is used to characterize on-chip antenna performance [Kim00a]. Note, that in actual system implementations, the antennas would only be matched for a limited frequency range; thus, G_a would only be equal to the actual gain over those frequencies.

Friis transmission formula assumes that the transmitting and receiving antennas are far enough apart such that they are in the *far-field region*. In the far-field region, only radiation terms (1/r) of the electromagnetic field dominate (power density ~ $1/r^2$), and the angular distribution of these terms is independent of distance [Wan86]. A *near-field region* also exists, where the reactive terms of the electromagnetic field dominate (i.e., the power density is complex). This reactive power refers to energy storage in the electric and magnetic fields; thus, wave propagation is not occurring. Finally, an *intermediate-field region* exists where radiation terms dominate; however, their angular distribution is a function of distance.

Multiple definitions abound for the boundaries between these regions. For an electrically short dipole antenna, whose length (L) is less than 0.33λ, the far-field criterion is [Bal97, Kim00a] as follows:

$$r \gg \frac{\lambda}{2\pi}. \tag{6.3}$$

These electrically short antennas are used in wireless interconnects, due to restricted die area for the antennas. If the >> symbol is interpreted as a single order of magnitude, the boundary between the intermediate- and far-field regions becomes as follows:

$$r > 1.6\lambda, \tag{6.4}$$

which agrees exactly with [Ban99]. Note that this criterion change as the antenna becomes electrically longer (i.e., L goes up, or frequency goes up), with the boundary shifting to $5L$ for $0.33\lambda < L < 2.5\lambda$ and $2L^2/\lambda$ for $L > 2.5\lambda$ [Ban99].

6.2.2 Types of Antennas

The ideal on-chip transmitting antenna would have an omnidirectional radiation pattern for the plane parallel to the wafer surface. Also, the transmitting antenna would have a large power handling capability. For clock distribution, in which there is only one transmitter whose position is fixed, the ideal on-chip receiving antenna would be directive, maximizing the antenna gain and minimizing interference and noise. Also, the receiving antenna should be area efficient since multiple receivers are included on chip.

Currently, dipole and loop antenna structures are being considered for single-chip wireless interconnects [Kim00a]. A horizontal dipole antenna is omnidirectional in the vertical plane perpendicular to the antenna axis. For a dipole antenna whose electrical length is less than approximately 0.85λ, the radiation resistance increases with antenna length [Bal97]. Also, the current distribution within the antenna increases with antenna length; thus, longer dipole antennas radiate more power. Half-wavelength dipole antennas (length = λ/2) are very common due to their radiation resistance being ~ 75 Ω, which is a traditional transmission-line characteristic impedance. The corresponding frequency at which the antenna is a half-wavelength long is the resonant frequency of the antenna.

For on-chip antennas, the antenna size is limited by the size of the chip. Therefore, to maximize the antenna's radiation while limiting the physical size of the antenna requires operating at higher frequencies (e.g., > 15 GHz), corresponding to smaller λ. For reference purposes, Table 6-1 shows the wavelength versus frequency for the following mediums: free-space, silicon dioxide, and silicon substrate. The dipole antenna length has been limited to 2 mm, corresponding to λ/10 and λ/5 at 7.4 and 15 GHz, respectively, in

Table 6-1 Wavelength in millimeters versus frequency for different mediums

Frequency	1 GHz	7.4 GHz	15 GHz	20 GHz	24 GHz
$\lambda_{free\text{-}space}$	300	40.5	20	15	12.5
λ_{oxide}	151	20.5	10.1	7.6	6.3
$\lambda_{silicon}$	87.2	11.8	5.8	4.4	3.6

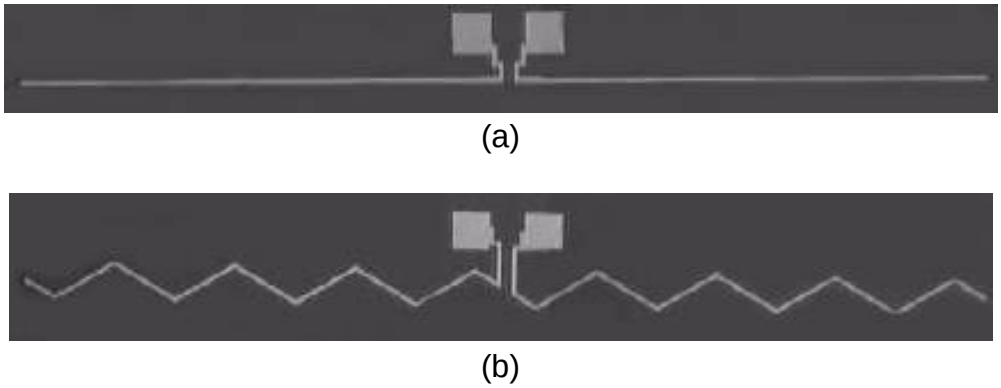


Figure 6-1 Die photograph of (a) linear and (b) zigzag dipole antennas.

silicon dioxide. Since the antenna is not operating at resonance (i.e., the length is not $\lambda/2$) then the antenna impedance has a reactive component. Therefore, this reactance has to be conjugately matched with the impedances of the transmitter and receiver.

Both linear and zigzag dipole antennas have been implemented. Die photographs of example antennas with pads are shown in Figure 6-1 [Kim00a]. The axial length of the antennas is 2 mm and the line trace width is 10 μm. For the zigzag antenna shown in Figure 6-1(b), the arm element length is 75 μm and the bend angle is 120^o, while the zigzag antennas implemented with clock receivers and transmitters have an arm element length of 80 μm and a bend angle of 30^o. Although the lateral field components cancel each other in a zigzag structure, the longitudinal components reinforce each other. Since the physical length of a zigzag antenna is longer than the linear dipole antenna, a zigzag dipole antenna

can have the same gain as a longer linear dipole antenna, while being more area efficient at the cost of added capacitance [Kim00a]. In other words, for the same axial length, the zig-zag dipole antenna will have higher gain than a linear dipole antenna.

Loop antennas are also being considered for wireless interconnects. A loop antenna whose total circumference (including multiple turns) is less than $\sim\frac{\lambda}{10}$ have a small R_r. Since the radiation resistance is much smaller than the loss resistance, loop antennas have very low efficiencies. This is a drawback of using loop antennas for clock transmission. To increase R_r, additional loops can be included. A horizontally oriented loop antenna is omnidirectional in the horizontal plane. Also, the loop antenna has an aspect ratio of 1, compared with the zigzag dipole antenna which has an aspect ratio of 25, indicating that loop antennas are more compatible to integrated circuit layout. Thus, a multi-loop antenna is a potential candidate for the transmitting antenna, provided that R_r can be sufficiently increased. As a first step towards evaluating this potential, a single-loop antenna with a 200-μm diameter and a 10-μm line width has been implemented [Kim00a].

6.2.3 Propagation Paths for On-Chip Antennas

Multiple propagation paths exist between two on-chip antennas. Figure 6-2 shows an illustration of a cross-section of a chip with antennas. These antennas are implemented in the top-level metal above an oxide layer. Located between the antennas are multiple metal test structures which interfere with the transmitted clock signal. Also, the chip will be flip-chip bonded onto a package substrate using solder balls. These ~100-μm diameter metal balls will interfere with the global clock signals. Finally, within the PC board there will be ground planes, which will again result in reduced antenna gain.

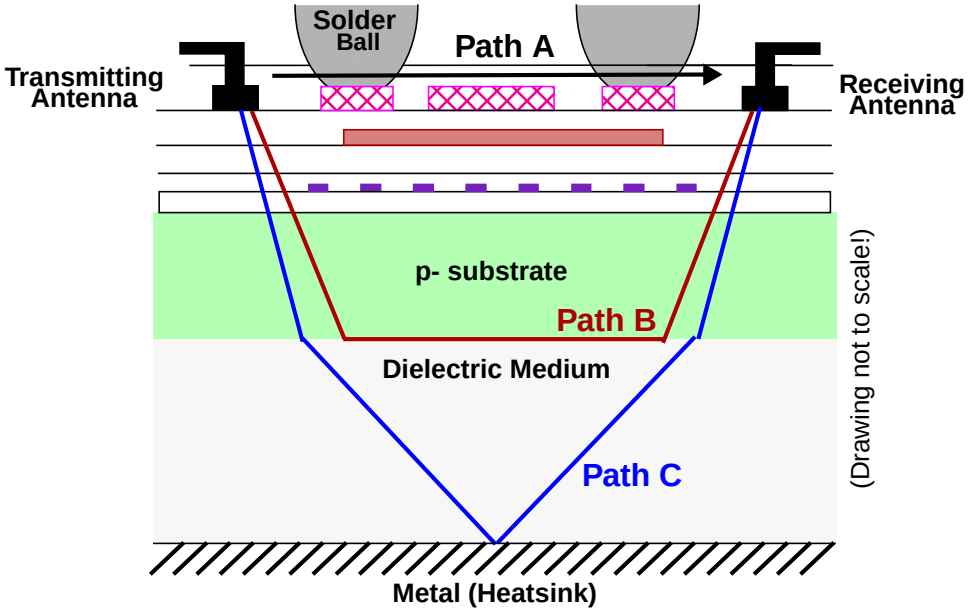


Figure 6-2 Cross-sectional illustration of chip for metal antennas with interference structures. Three possible signal paths between antennas--path A is direct path, path B is substrate surface wave, and path C is substrate reflection.

Beneath the oxide is the substrate. This substrate then is connected to a heatsink, which is used to remove the heat from the microprocessor. Experimental results, though, show that this situation is not very conducive to on-chip signal transmission for substrate resistivity less than ~ 20 Ω-cm. Instead, if a dielectric layer is placed between the substrate and heatsink, the antenna gain can increase by as much as 8 dB [Kim00a, Guo01], depending on the dielectric material and its thickness. Since heat still needs to be removed from the chip, this dielectric layer has to be thermally conductive. A possible material which meets both criteria is aluminum nitride (AlN) [Guo01]. Aluminum nitride has a thermal conductivity approximately the same as that of silicon and about 10 times that of glass, and its dielectric constant is 8.5.

Due to the interference structures, the direct path from one antenna to another, labeled path A in Figure 6-2, will be very attenuated for on-chip wireless interconnection. This direct path is also referred to as a surface wave. The gain of this path will depend on

the interference structures between the antennas. Unfortunately, a wireless interconnect designer has no control over these layers, and, thus, can't predict the performance for the antenna pair. Another path for signal propagation is through the substrate and back-layer dielectric. These mediums are unused in normal system design, and therefore are well-suited for wireless interconnects. These mediums can actually support two modes. One is a reflected path, where the signal refracts through the substrate and dielectric layer, bounces off of the back-side metal layer, and then travels back up to the receiving antenna. This path is labeled path C. A third path is the substrate surface wave (also known as a lateral wave), labeled path B. This wave is generated from antennas which have finite beam widths [Kim00a] (i.e., it does not exist for plane waves). Analyses of this path are contained in [Boa82] and [Kim00a]. Experiments show that for the case when no interference structures are present, the gain through the substrate paths (B and C) can be comparable to the gain through the direct path A. The relative strength of paths B and C depends on the type and size of the underlaying dielectric medium [Guo01]. Much greater detail on the modeling of each of these paths is contained in [Kim00a, Guo01].

6.3 Antenna Characteristics in 0.25-μm CMOS

Figure 6-3 shows a photo-illustration of a test chip used to characterize both antennas and antennas with LNA, and to demonstrate an on-chip wireless interconnect. This test chip was fabricated in a standard 0.25-μm CMOS process and is approximately 7.8 mm^2. The 0.25-μm LNA and frequency divider presented in chapters 2 and 3 have also been implemented in this test chip. Located on the far left and far right are a pair of linear dipole antennas, which are used to characterize the antennas as well as to transmit to the receiver circuitry. Also, on the right is an LNA with an integrated antenna, while on the left is a

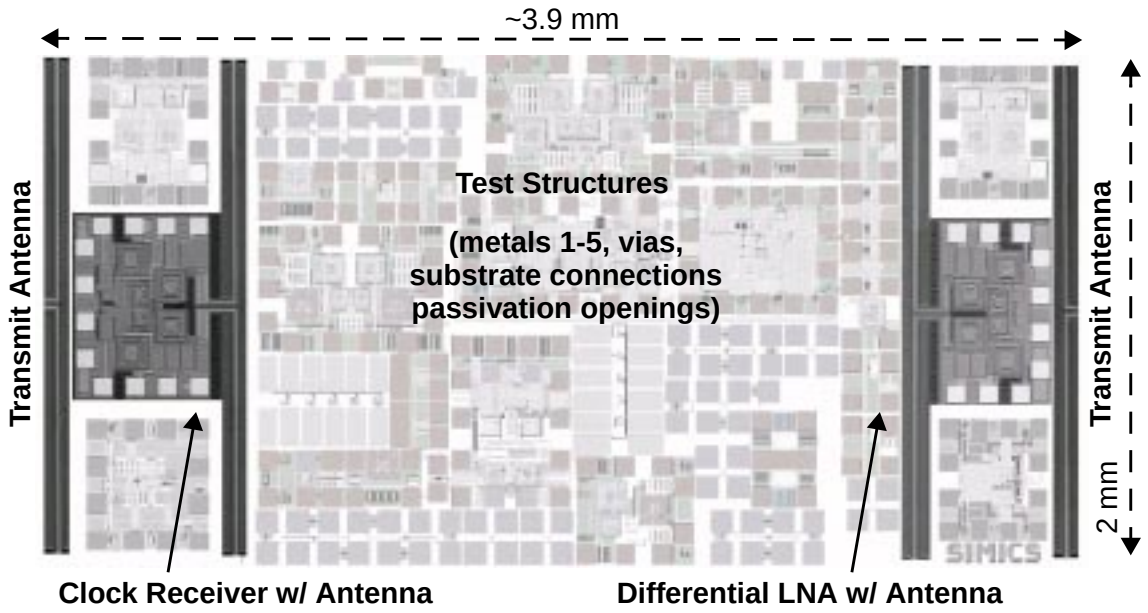


Figure 6-3 Photo-illustration of 0.25-μm test-chip including antenna pair, antenna with LNA, and antenna with clock receiver.

clock receiver with an integrated antenna. Located between the antennas are test structures which interfere with the clock transmission and reception. These test structures contain multiple metal layers, vias, substrate connections, and passivation openings.

6.3.1 Measured Characteristics for Antennas

A test setup for antenna characterization utilizing a network analyzer has been developed [Kim00a], and is shown in Figure 6-4. This setup converts the unbalanced signals from the network analyzer to balanced signals used to excite the antennas. Semi-rigid cables are used to increase measurement reliability. Also shown is a cross-section of the on-wafer measurement setup. The dies are mounted on a glass slide, which is then placed on various insulators with κ's ranging from 2 (wood) to 8.5 (AlN).

Figure 6-5(a) shows the measured transducer and transmission gain from 6 to 18 GHz between two on-chip linear dipole antennas which are separated by 3.9 mm. The

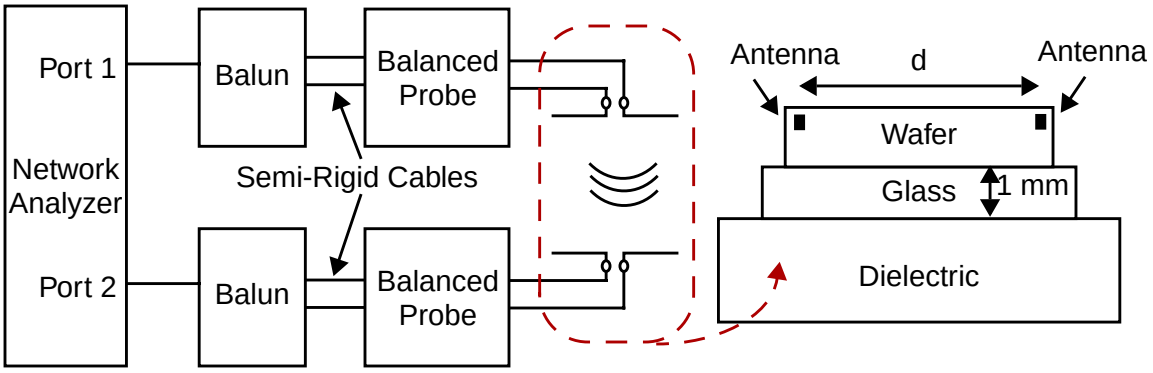


Figure 6-4 Measurement setup used to characterize on-chip antenna pair. On-wafer measurements are performed with the die mounted on a glass slide above a dielectric insulator.

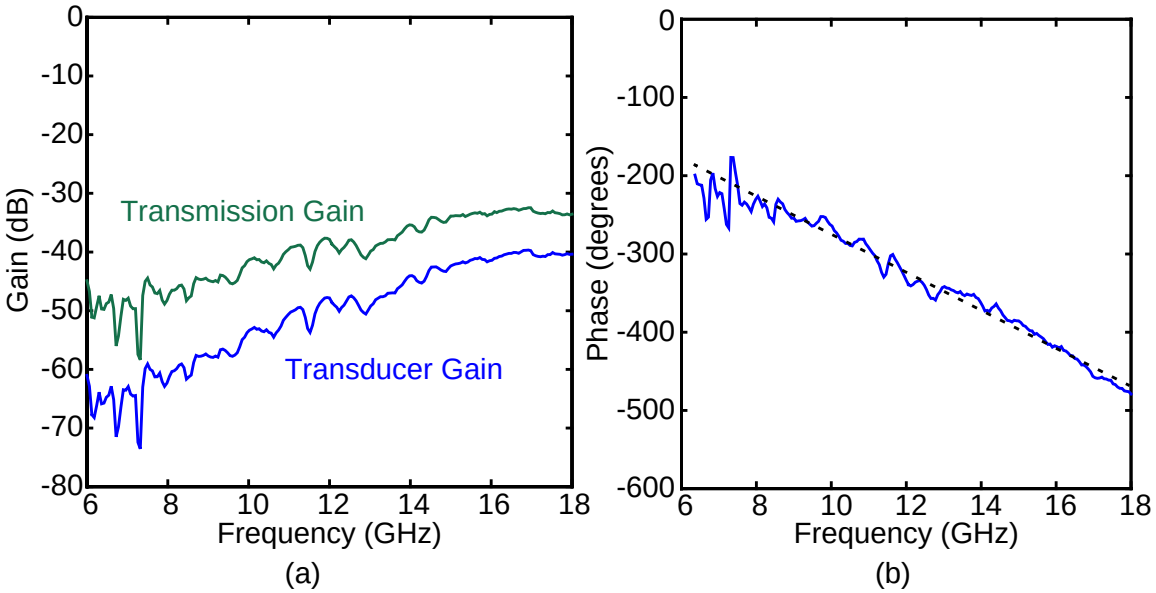


Figure 6-5 (a) Transducer and transmission gain of linear dipole antenna pair.
(b) Phase versus frequency for linear dipole antenna pair.

antennas are implemented in metal 5 and separated from the substrate by ~7 μm of oxide. These results are for a substrate resistivity of ~ 8 Ω-cm. As can be seen, the antenna is more efficient at higher frequencies, or when signal wavelengths are smaller. A transducer "gain" of -64 dB is attained at 7.4 GHz, while the transmission gain is -49 dB. The large difference between the transducer and transmission gain is due to the antenna impedance being significantly different than the 100-Ω differential impedance (i.e., differential voltage over differential current). Since the 0.25-μm LNA, presented in section 3.4, is

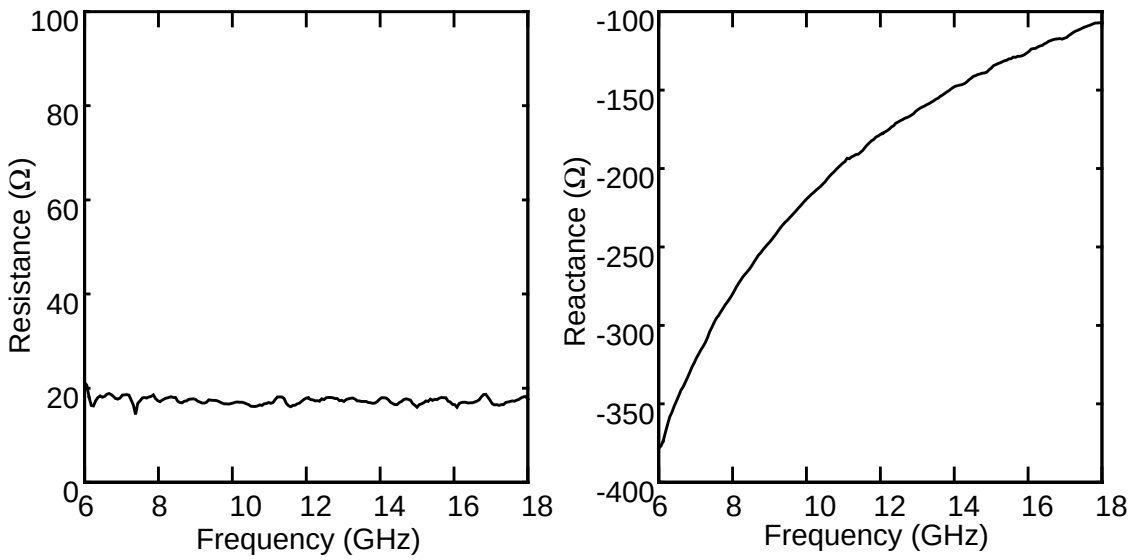


Figure 6-6 Antenna impedance versus frequency for linear dipole antenna.

matched differentially to 100 Ω, the mismatch for the antennas in the measurement system is virtually the same as when the antenna is integrated with the LNA. The measured antenna impedance, shown in Figure 6-6, at 7.4 GHz is approximately 20-j300 Ω. Comparing this impedance to 100 Ω, the total mismatch loss for the antenna pair can be calculated to be 15 dB, using equations (5.3) and (5.4).

The reason for such a low antenna impedance is still not known for certain. Previous antenna implementations indicate that this same antenna should have an impedance closer to 100 Ω [Kim00a]. A potential reason for this low impedance is the effect of interference structures, including metal dummy patterns for chemical-mechanical polishing, on antenna impedance. What *is* known for certain, is that a 15-dB mismatch loss is unacceptable. Clearly, better techniques are required to predict the antenna impedance, so that proper matching circuitry can be designed. Alternatively, adjustable matching networks can be designed to allow for the receiver input match to be tuned to account for antenna impedance variations.

Figure 6-5(b) shows the measured phase versus frequency for the voltage ratio between a receiving and transmitting antenna pair. With 50-Ω transmission lines at both ports of the network analyzer, this phase is defined as follows:

$$\phi = angle\left(\frac{V_2}{V_1}\right) = angle\left(\frac{(a_2 + b_2)\sqrt{Z_{o2}}}{(a_1 + b_1)\sqrt{Z_{o1}}}\right)\Bigg|_{a_2 = 0} = angle\left(\frac{S_{21}}{1 + S_{11}}\right), \quad (6.5)$$

where a_i and b_i are the normalized incident and reflected voltage waves at each port. The phase delay decreases linearly with frequency ($\phi = -\omega l/c_{eff}$), indicating wave propagation rather than some type of lumped element RC coupling [Kim00a]. Finally, the transducer gain between two sets of pads was measured to be approximately 10 dB less than the measured antenna gain. Thus, these two facts together show that the signal coupling is due to wave propagation, and that these waves are launched much more efficiently from the antennas than from just the pads.

6.3.2 Integrated Antenna with LNA

An integrated linear dipole antenna with an LNA was included on the 0.25-μm test chip, to study the interaction between the antenna and LNA [Flo00a]. The measurement setup used to characterize the antenna/LNA combination was identical to that in Figure 6-4. The S-parameters of the antenna pair and an antenna pair with an LNA connected to the receiving antenna were measured. Figure 6-7(a) shows the measured transducer gain between the antenna pair and the antenna with LNA for a separation distance of ~ 3.3 mm. As can be seen, the LNA is providing gain for frequencies below ~ 9 GHz. The transducer gain of the antenna pair can then be de-embedded from the antenna with LNA measurement to extract the LNA gain. This result is shown in Figure 6-7(b), along with the

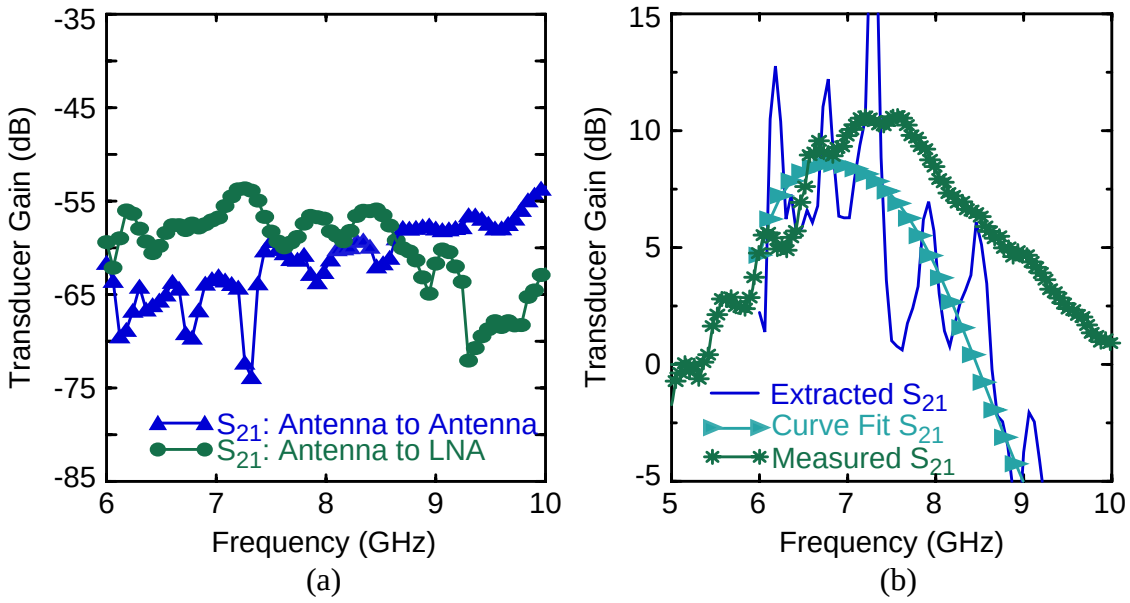


Figure 6-7 (a) Measured transducer gain between antenna pair and antenna pair with LNA. (b) Extracted and measured gain of LNA.

measured gain of the LNA from section 3.4. The antenna and antenna-with-LNA gain measurements are noisy due, in part, to insufficient averaging on the network analyzer and, in part, to the interference structures located between the antennas. To indicate the qualitative trend of the antenna with an LNA measurement, a curve fit is included. These results show that the LNA is amplifying the signal received by the antenna.

6.4 Wireless Interconnect in 0.25-µm CMOS

Figure 6-8 contains a die photograph of the clock receiver with an integrated dipole antenna. The size of the receiver including the antenna and "unused" portion on either side of the receiver is 0.7 x 2 mm^2, while the size of the receiver alone (excluding pad area) is 0.4 x 0.5 mm^2. Since the clock receiver is fully differential, the receiver layout should be symmetric for each half-circuit of the receiver, including all components, supply voltage lines, and pads. This avoids any systematic errors being introduced from layout

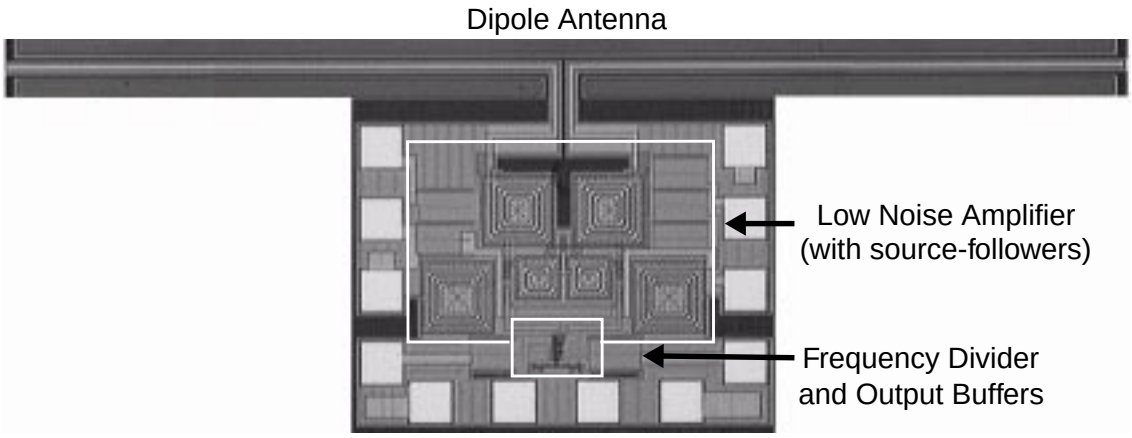


Figure 6-8 Die photograph of 0.25-μm clock receiver with linear dipole antenna.

mismatch. Additionally, multiple substrate connections should be included for both the LNA and divider. In particular, to minimize any substrate crosstalk, a guard-ring structure should separate the LNA from the divider. Finally, the LNA and buffer should have a separate supply voltage from the frequency divider.

Figure 6-9(a) shows the measurement setup used to demonstrate a single-receiver wireless interconnect. A 7.4-GHz global clock signal is externally generated and then amplified to 21 dBm to overcome the low antenna transducer gain. This signal is converted to a balanced signal and injected to the on-chip transmitting antenna. The global clock signal propagates 3.3 mm across the chip to the receiver, whose output is measured using an oscilloscope. Figure 6-9(b) shows plots of the input voltage (before the external amplifier) to the transmitting antenna and the output voltage for the wireless clock receiver. As can be seen, a 925-MHz (7.4 GHz divided by eight) local clock signal is generated, demonstrating the operation of the single-receiver on-chip wireless interconnect for clock distribution. The reduced voltage swing at the output is from driving a 50-Ω load. As inferred from the measured antenna-pair transducer gain of -64 dB, the received signal level is -43 dBm at the LNA input. Since the receiver would not lock to the

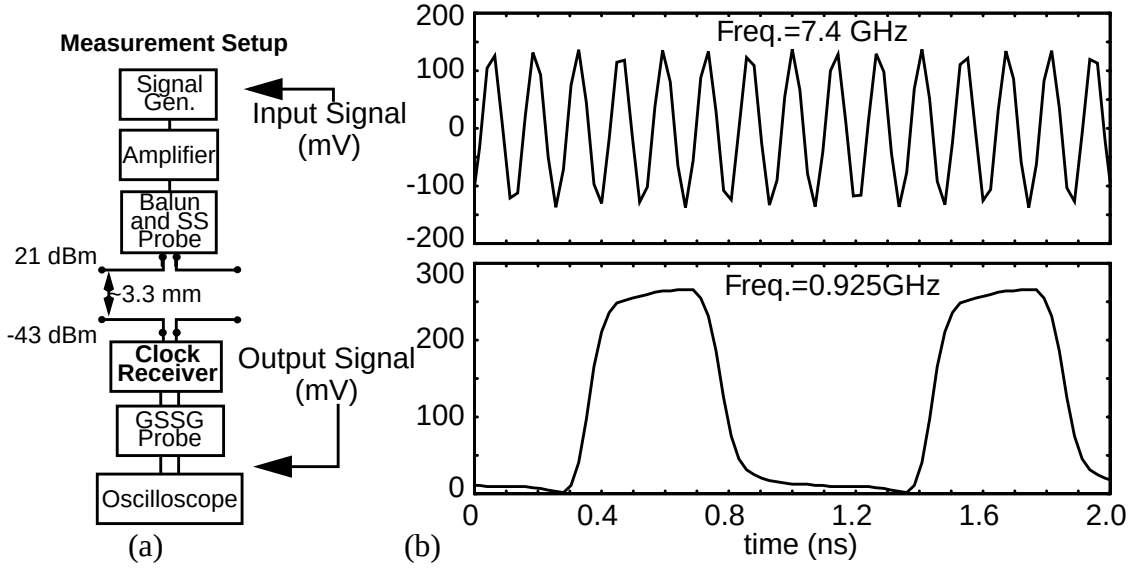


Figure 6-9 (a) Measurement setup used to characterize clock receiver. (b) Input and output waveforms for the clock receiver (f_{in}=7.4 GHz and f_{out}=7.4 GHz/8 = 925 MHz) for a interconnection distance of 3.3 mm.

transmitted signal for lower input power levels, the minimum detectable signal of the receiver is -43 dBm. The receiver consumes 62.5 mW from a 2.5-V supply.

This result is the first demonstration of an on-chip wireless interconnect. A 7.4-GHz global clock signal is successfully received over a 3.3-mm distance with interference structures located in between the antennas, and a 925-MHz local clock signal is generated. Also, this result is the first to integrate antennas and CMOS circuitry on a single chip. Therefore, plausibility of a wireless system has been demonstrated using a standard 0.25-μm CMOS technology at ~8 GHz. Based on this result, superior performance is expected by using a more advanced CMOS technology. This allows the operating frequency to increase, improving the efficiency of the antennas, which in turn allows longer interconnection distances.

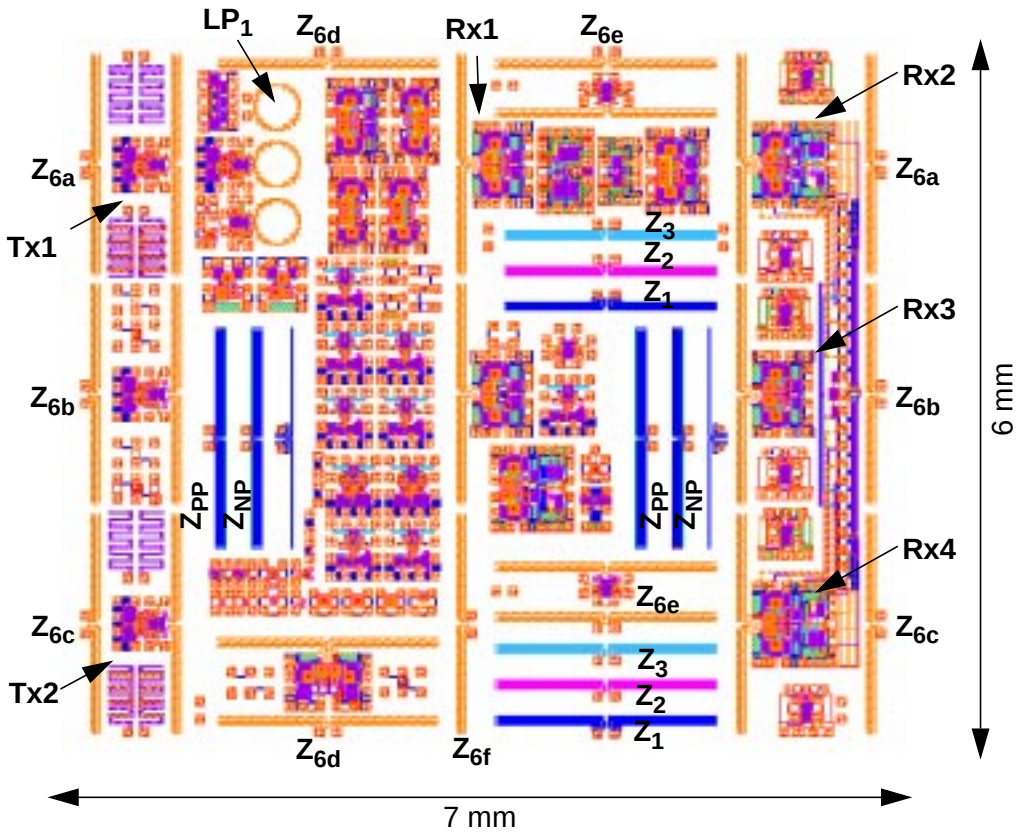


Figure 6-10 Layout of UMC test-chip showing locations of relevant zigzag antennas (Z_x), loop antenna (LP_1), clock transmitters (Tx), and clock receivers (Rx).

6.5 Antenna Characteristics in 0.18-µm CMOS

6.5.1 Chip Implementation

Based on the results achieved in the 0.25-µm CMOS test chip, a test chip was implemented in a 0.18-µm CMOS technology with copper interconnects. This technology was obtained from UMC as part of the SRC Copper Design Challenge, sponsored by the Semiconductor Research Corporation (SRC), Novellus, SpeedFam-IPEC, and UMC. The substrate resistivity is 15-25 Ω-cm. Six layers of copper interconnect were provided.

Multiple antenna test structures, LNAs, frequency dividers, clock receivers, and clock transmitters have been included in this test chip. Figure 6-10 shows the layout of the

UMC test-chip, whose area is 7 x 6 mm^2. The locations of relevant zigzag antennas (Z_x) and the loop antenna (LP_1) have been noted. Clock transmitters (Tx1, Tx2) and receivers (Rx1-Rx4) have been labeled as well. Located in between the antennas are test structures which interfere with the clock transmission and reception. These test structures contain multiple metal interconnects, vias, substrate connections, passivation openings, and metal-fill patterns (not shown) for metal layers 1 through 6. Therefore, the density of structures between the antennas is high.

6.5.2 Antenna Descriptions

The majority of the antennas implemented are 2-mm long zigzag dipole antennas, labeled Z_X in Figure 6-10. The zigzag antennas, illustrated in Figure 6-11, have a 10-µm trace-width, an 80-µm arm element length, and a 30^o bend angle. These values were based on the best results currently available from antenna design experiments [Kim00b]. Antennas Z_{6a} to Z_{6f} are implemented in metal 6 at various locations throughout the chip, with spacings of d={6.7, 6.7, 6.7, 5.7, 4.3, 3.2} mm, for antenna pairs $Z_{\{6a, 6b, 6c, 6d, 6e, 6f\}}$ respectively. The distance from metal 6 to the substrate is ~7.2 µm. Also, different metal layers were used to fabricate the antennas to examine their dependence on antenna gain. These antennas are labeled Z_1, Z_2, and Z_3, and are separated by 3.6 mm.

Two antennas are evaluated for use in the transmitter--a zigzag dipole antenna and a loop antenna (LP_1) which has an omnidirectional in-plane radiation pattern [Bal97]. The

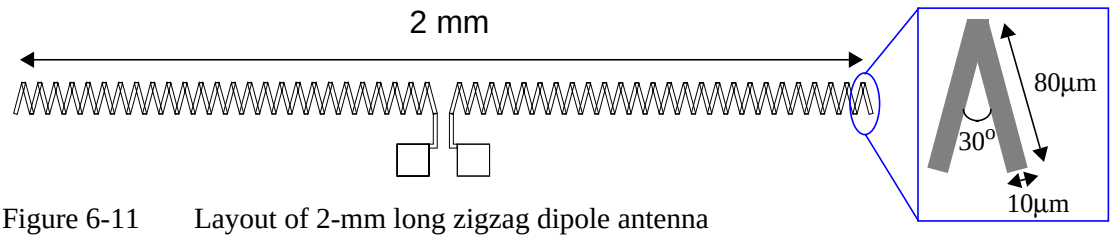


Figure 6-11 Layout of 2-mm long zigzag dipole antenna

zigzag antenna is identical to the antenna used for the receiver, while the loop antenna has a diameter of 200 µm and a trace-width of 10 µm, implemented in metal 6. The gain from a loop antenna to zigzag antenna will be analyzed for different distances and angles.

This test chip also includes zigzag antennas in direct contact with the substrate, where the zigzags have the same dimensions as presented above. This idea is motivated by the fact that there will be many on- and off-chip metal interference structures between the antennas. As shown in Figure 6-2 and discussed in section 6.2.3, the interference structures can severely attenuate the direct path between two metal antennas. A more suitable medium for wireless interconnects is the substrate. Figure 6-12 shows a cross-section of a chip containing substrate antennas. If the substrate and back-side dielectric are being exploited, then the antennas do not need to be implemented in top-level metal. Instead, the antennas are implemented with n-plus in p-substrate and with p-plus in n-well. This can potentially alleviate metal routing constraints around the antenna.

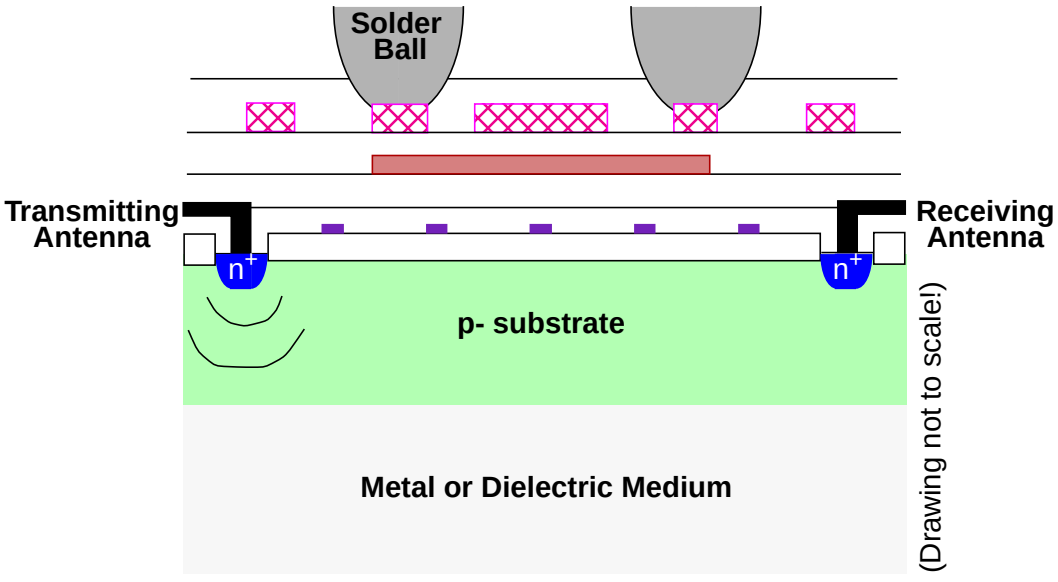


Figure 6-12 Cross-sectional illustration of antennas in direct contact with substrate.

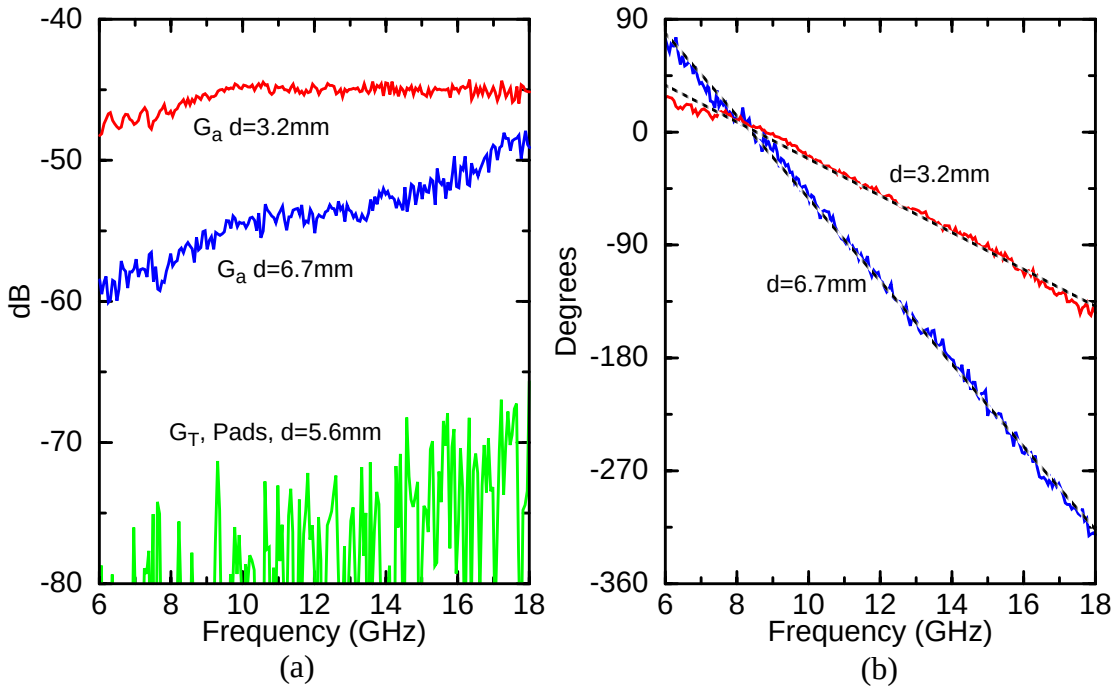


Figure 6-13 (a) Zigzag-zigzag transmission gains for d=6.7 mm (Z_{6b}) and 3.2 mm ($Z_{6c\text{-}6f}$). Also shown is the pad transducer gain ($|S_{21}|^2$)at d=5.6 mm for reference. (b) Phase versus frequency of voltage wave for d=6.7 and 3.2 mm.

6.5.3 Measured Antenna Characteristics

The balanced measurement setup shown in Figure 6-4 was used to characterize the antenna pairs. Figure 6-13(a) shows the measured zigzag-zigzag transmission gain (G_a) versus frequency for 6.7- and 3.2-mm separations, corresponding to antenna pairs Z_{6b} and $Z_{6b\text{-}6f}$, respectively. The gain increases with frequency and decreasing separation. At 15 GHz, G_a is -53 and -45 dB for 6.7- and 3.2-mm separations, respectively. Also shown is the gain ($|S_{21}|^2$) between two sets of pads separated by 5.6 mm, which is about 20 dB below the transmission gain at 15 GHz. For this measurement situation, the pad-to-pad gain is close to the instrument noise floor. The phase delays between the voltages at the receiving and transmitting antennas are shown in Figure 6-13(b). The phase delay decreases linearly with frequency, again indicating wave propagation rather than some type of lumped-element RC coupling. This fact, along with the low pad-to-pad gain, show

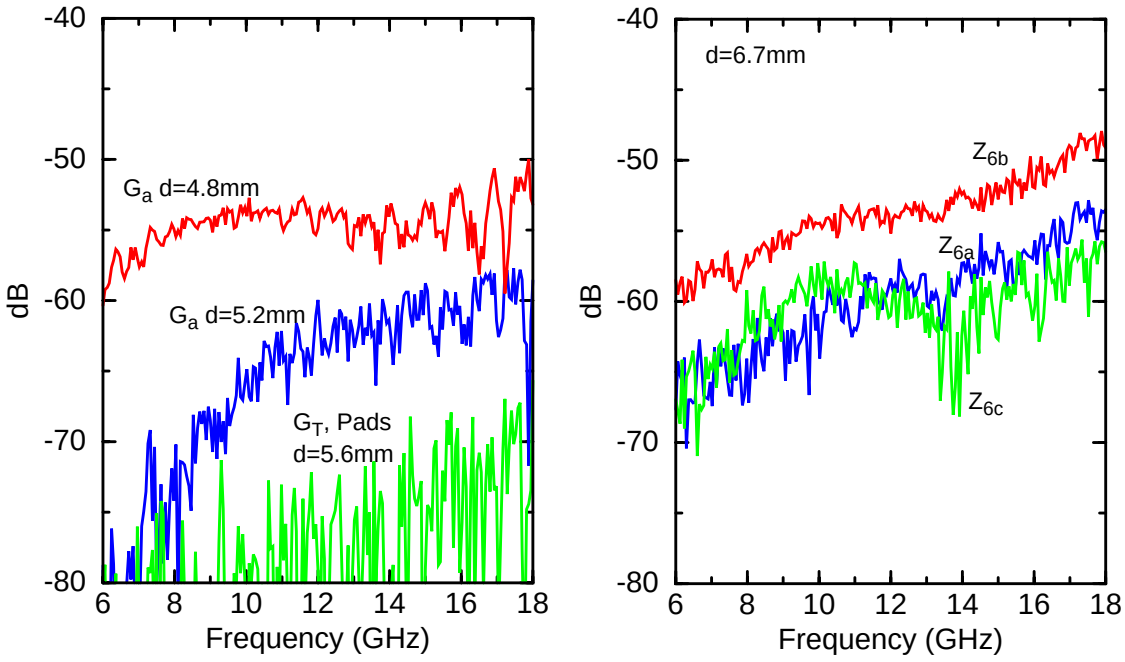


Figure 6-14 (a) Loop-zigzag transmission gains for d=5.2 (LP_1-Z_{6f}) and 4.8 mm (LP_1-Z_{6a}). Also shown is the pad transducer gain ($|S_{21}|^2$) at d=5.6 mm for reference. (b) Zigzag transmission gains for metal-6 antennas ($Z_{6a,6b,6c}$) at d=6.7 mm, demonstrating the effect of interference structures on gain.

conclusively that the signal is propagating from one antenna to the other, and that these waves are launched much more efficiently from the antennas than from the pads alone.

Figure 6-14(a) shows G_a versus frequency for a loop-zigzag antenna pair at 5.2- and 4.8-mm separations (corresponding to antenna pairs LP_1-Z_{6f} and LP_1-Z_{6a}, respectively). At 15 GHz, G_a is -58 and -54 dB, respectively, which is less than the zigzag-zigzag gains. These results are promising, though, and show that at high enough frequencies, loop antennas are useful for the transmitting antennas.

Figure 6-14(b) shows G_a versus frequency for three pairs of zigzag antennas. Each pair is separated by 6.7 mm, corresponding to antennas $Z_{6a,6b,6c}$. These results demonstrate the effect of interference structures on antenna gain. As can be seen from Figure 6-10, each pair has different types and densities of metal and active structures located in

between. The transmission gain changes by 5 to 10 dB, depending on the antenna and frequency. Also, the antennas have slightly different impedances (not shown), since the reflection coefficient is a function of the metal structures reflecting the transmitted signal back into the antenna. This shows that the structures located around the antenna affect the antenna performance. The implication on system design is that this degradation in signal level has to be accounted for when estimating the worst-case signal-to-noise ratio. Also, this shows the need for electromagnetic simulation tools which can be used to try to estimate the effects of these structures beforehand, allowing design rules to be developed. Much greater analysis of this problem is contained in [Yoo00, Kim00a, Kim00b].

Figure 6-15(a) shows the reflection coefficients of the loop and zigzag antennas on an impedance Smith chart, while Figure 6-15(b) shows the measured antenna impedance for a zigzag (Z_{6b}) antenna and a loop (LP_1) antenna. The zigzag impedance is ~100 Ω with a capacitive reactance; the loop impedance is ~50 Ω with an inductive reactance. The mismatch loss between the receiving zigzag antenna and the LNA input (which was matched to ~100 Ω) is approximately 0.3 dB at 15 GHz. Therefore, virtually all of the power from the receiving antenna is transferred to the LNA.

Figure 6-16(a) shows the measured antenna gain for zigzag dipole antennas implemented in either metal 1, 2, or 3. At 15 GHz, the gains are -43, -49, and -49 dB, for antennas Z_1, Z_2, and Z_3, respectively. The gain for the antennas in metal 1 is about 5 dB greater than that in metals 2 and 3 for frequencies above ~12 GHz. The antennas in metals 2 and 3 have nearly the same characteristic, where the gain decreases and then plateaus with frequency. Finally, the gain for these antennas at 3.6-mm separation is close to the gain of the metal-6 antenna, Z_{6f} (-45 dB at 3.2 mm). More work is required to understand these effects, both with and without metal interference structures present.

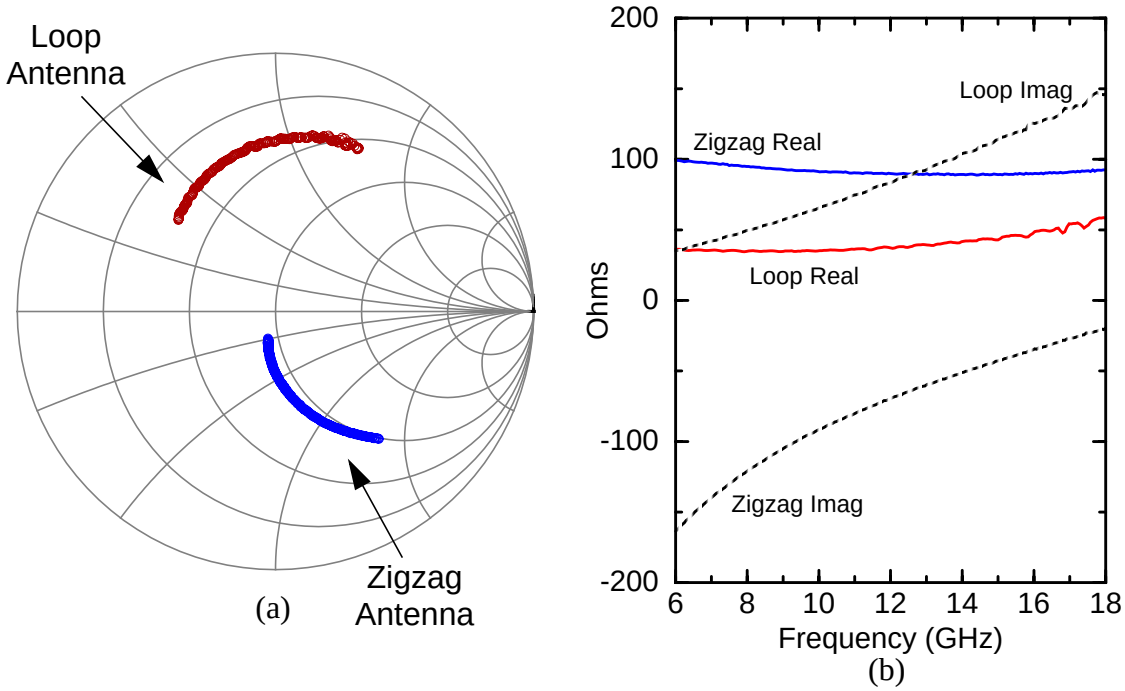


Figure 6-15 (a) Impedance smith chart showing reflection coefficients of zigzag and loop antennas (Impedances are normalized to 100 Ω). (b) Antenna impedance for zigzag and loop antennas (Z_{6b} and LP_1).

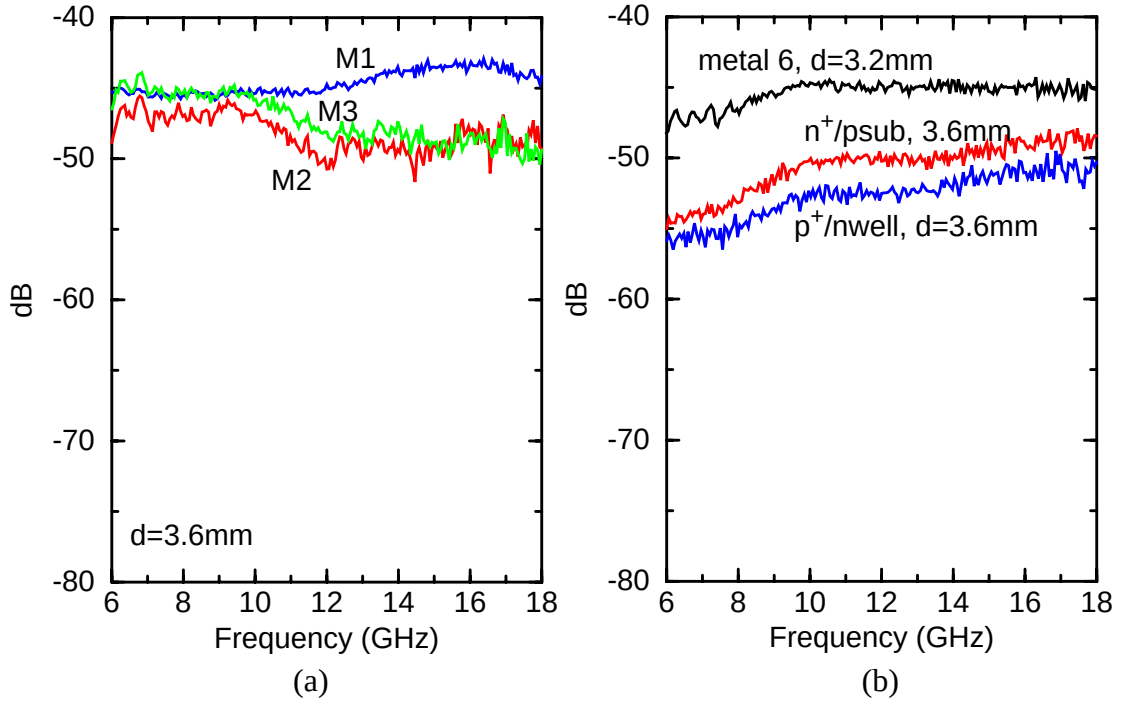


Figure 6-16 (a) Zigzag transmission gains at d=3.6 mm for antennas in metals 1, 2, or 3. (b) Zigzag transmission gains at d=3.65 mm (Z_{pp}, Z_{np}) for antennas implemented in direct contact with substrate, with n-plus in p-sub and p-plus in n-well. Metal-6 antenna at d=3.2 mm is shown for comparison purposes.

Table 6-2 Comparison between measured and expected antenna characteristics, 0.18-μm

Antenna Pair	Parameter at 15 GHz	Expected	Measured
Zigzag to Zigzag	Gain (d=6.7mm)	-48 dB	-53 dB
	Impedance (Zigzag)	125 - j55 Ω	89 - j43 Ω
Loop to Zigzag	Gain (d=5.2mm)	-51 dB	-58 dB
	Impedance (Loop)	30 + j80 Ω	43 + j114 Ω

Figure 6-16(b) shows the measured gain versus frequency for the substrate antennas. These substrate antennas are implemented in n^+ in p-substrate and p^+ in n-well, overlaid with metal 1 and multiple contacts. At 15 GHz for a 3.65-mm separation, the gains for a n-plus antenna implemented in p-substrate and for a p-plus antenna implemented in n-well are -51 and -49.5 dB, respectively. The gains are between 7 to 3 dB less than that for the metal-6 zigzag (d=3.2 mm), for frequencies between 6 to 18 GHz, respectively. This result suggests that substrate antennas can be used for wireless interconnection at frequencies above 18 GHz. Further feasibility studies are required

A comparison between the expected and measured antenna characteristics at 15 GHz is shown in Table 6-2. The expected characteristics were extracted from the results in [Kim00a]. These characteristics agree remarkably well, with the difference attributed to the interference structures located between the antennas. While this result is encouraging, the fact that the results on the 0.25-μm test chip for very similar antennas did not match is equally disturbing. In particular, the impedance of the 0.25-μm antennas was about one fifth of the 0.18-μm antenna impedance, resulting in a large mismatch. Both test chips have metal-fill patterns which are required to maintain chemical-mechanical polishing (CMP) uniformity. One difference between the chips is that the 0.18-μm chip allowed for

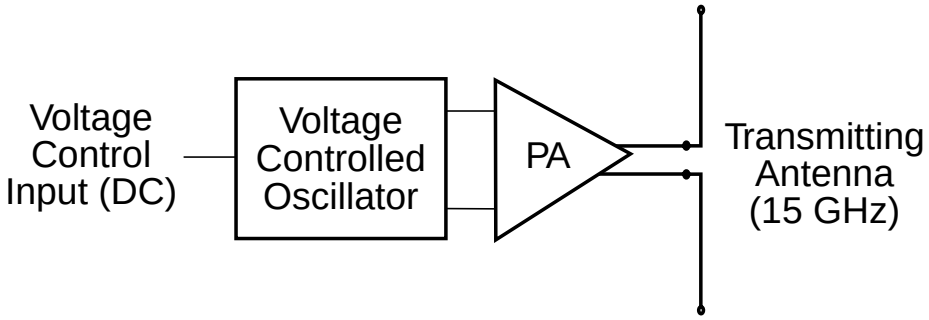


Figure 6-17 Block diagram of clock transmitter for 0.18-μm test chip.

these fill patterns to be blocked around the antenna, while no blocking was used in the 0.25-μm chip. Currently, it is not known whether this difference can account for the difference in the impedance. More experimental and modeling work is required to understand these discrepancies, since predicting the antenna performance is critical to a working wireless interconnect system.

6.6 Wireless Interconnects in 0.18-μm CMOS

6.6.1 Clock Transmitter

Figure 6-17 shows a simplified block diagram for the clock transmitter. The 15-GHz signal is generated using a differential voltage-controlled oscillator (VCO). The VCO is required to have low phase noise to decrease the local clock jitter. The signal from the VCO is then amplified by a two-stage output power amplifier and delivered to the transmitting antenna. In the final clock distribution system implementation, the VCO will be phase-locked to an external reference. However, to ease the implementation requirements for this chip, the transmitter was operated open-loop, where the frequency of the VCO was controlled directly with its dc input. This clock transmitter was primarily designed by Chih-Ming Hung and characterized by the author. Accordingly, the basic circuit design will only be briefly reviewed, specifically for the VCO where the interested

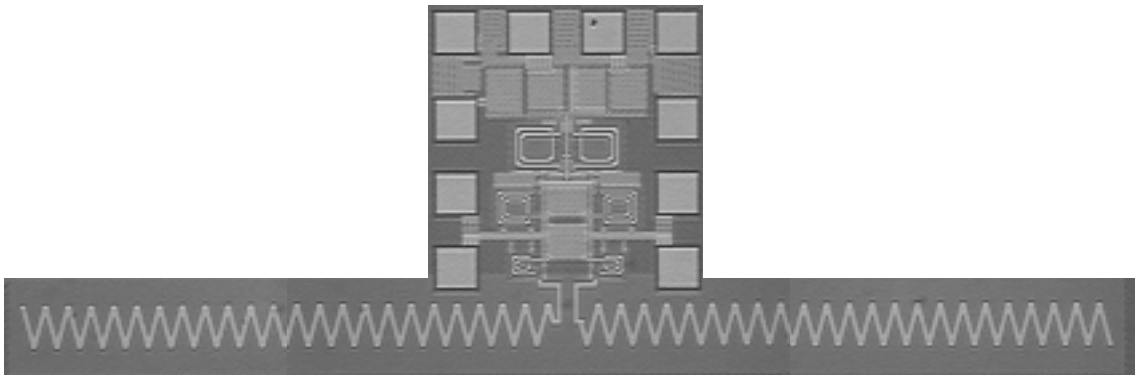


Figure 6-18 Die photograph of 0.18-μm clock transmitter with zigzag dipole antenna.

reader can refer to [Hun00a]. Instead, the discussion will focus on the measured characteristics and their implication for wireless interconnect design.

Figure 6-18 shows a die photograph of the clock transmitter with a zigzag antenna. The size of the transmitter, including the "unused" portions on either side of the circuit, is 0.64x2 mm^2, while the active areas (excluding pads) is 0.4x0.29 mm^2. The layout is symmetric left-to-right. Multiple substrate connections are included throughout the circuit.

6.6.2 Voltage Controlled Oscillator

Figure 6-19 shows a schematic of the VCO and PA. Cross-coupled transistors, M_1 and M_2, form a positive feedback, providing negative resistances to the LC tanks. Instead of a conventional tail-current source, a PMOS transistor, M_7, is placed at the bottom to perform a comparable function. This allows the VCO core output to be dc coupled to the PA. Simulation shows that when using this configuration, the phase noise contributed from the noise present at the gate of M_7 is lower as compared to that of a conventional current source [Hun00c]. To generate the same negative resistance with a given current, the required width of a PMOS transistor is larger than that of an NMOS transistor, due to

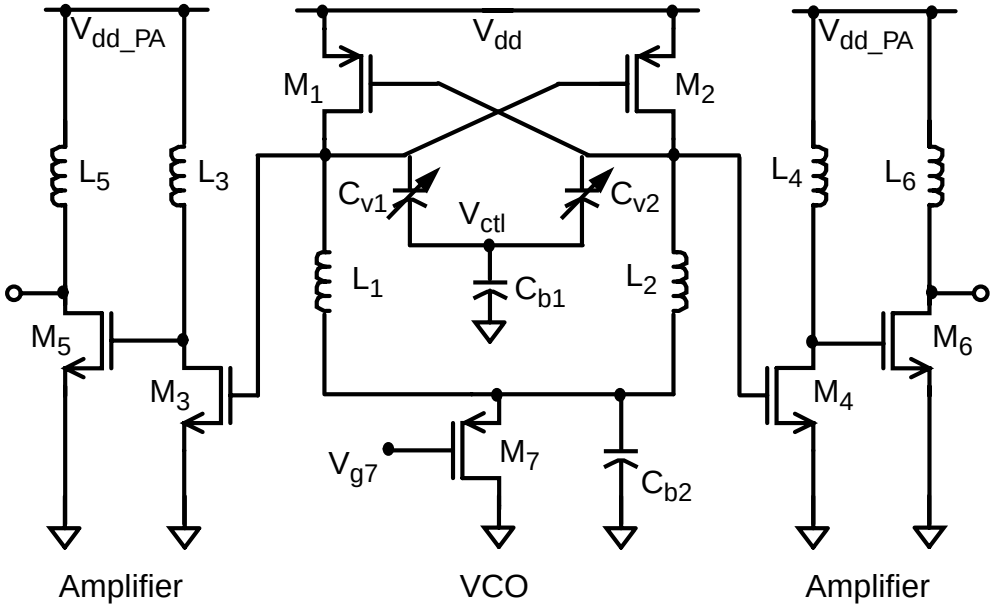


Figure 6-19 Schematic of the VCO and output amplifier.

lower mobility. This implies that the total gate area is larger if PMOS is used for the oscillator. Since 1/f noise is approximately inversely proportional to the gate area, the close-in phase noise can be reduced. Furthermore, PMOS transistors have much lower hot-carrier noise, according to [Che90]; thus, the far-out phase noise would also be improved. Hence, PMOS transistors are exclusively used in this VCO design [Hun00a].

The inductance of both L_1 and L_2 was designed to be 0.33 nH, while measurements reveal an inductance of 0.41 nH. This increase in inductance as well as increased capacitance from the transistors, as presented in section 3.5.3, decreased the VCO operating frequency from ~21 GHz to 15 GHz. The inductors were implemented with metal 5 and 6 layers shunted together above a patterned ground shield. As mentioned in Chapter 3, this improves the inductor Q by providing a low resistance path to ground for capacitively coupled current. The area of the inductor is 70.6x70.6 μm^2, and the metal spacing, width, and number of turns are 2.2 μm, 6.6 μm, and 1.75, respectively. The expected inductor Q

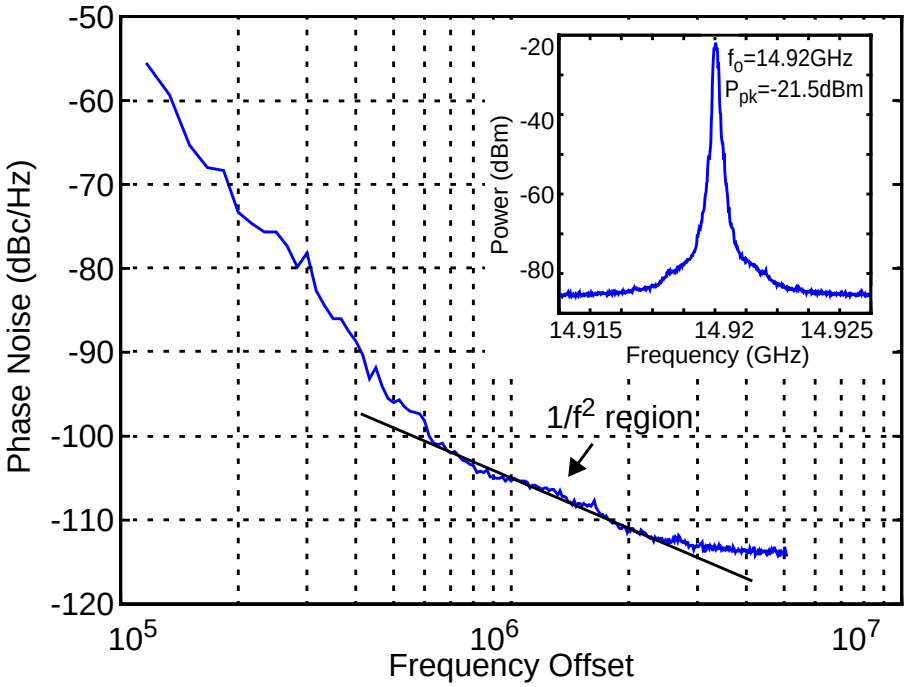


Figure 6-20 Single-sideband plot for 0.18-µm VCO with output spectrum inset.

was 32.9, while the measured Q was ~10. This reduction in Q was due to the thinning of the top-layer metals, once again discussed in section 3.5.2. The varactor is implemented using an accumulation-mode high-Q MOS capacitor [Hun98]. Measurements show that the varactor Q is approximately 47 at 15 GHz.

A VCO test structure consisting of the VCO core plus a single-stage 50-Ω output buffer was connected to a spectrum analyzer, yielding the output single-sideband phase-noise plot and spectrum shown in Figure 6-20. With V_{ctl} = 1.2 V, the measured center frequency is 14.92 GHz, with an output power level of -21.5 dBm. The VCO core consumes 7.2 mW from a 1.5-V supply. The phase noises at 1-MHz and 3-MHz offsets are -105 and -113 dBc/Hz, respectively. Finally, an oscillation frequency versus control voltage plot is shown in Figure 6-21. The tuning range is 690 MHz, for V_{ctl} between 0 and 1.8 V. The linear portion of this curve reveals a VCO gain of approximately 600 MHz/V.

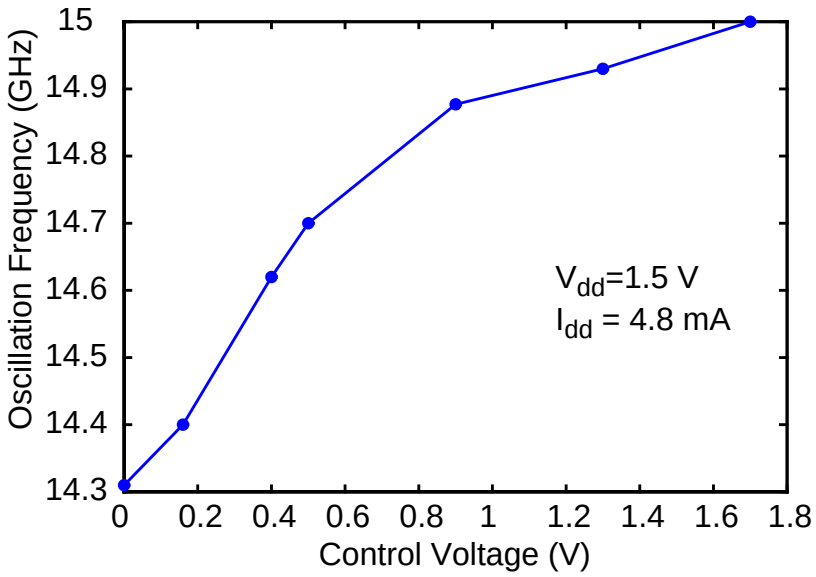


Figure 6-21 Measured tuning range for 0.18-µm VCO.

Table 6-3 shows a comparison between the expected and measured VCO results. The overall Q of the LC tank is the major limiting factor of the phase noise performance, where the tank consists of L_1, L_2, C_{v1}, C_{v2}, the gate and drain capacitances of M_1 and M_2, and the gate capacitances of M_3 and M_4. Since the measured Q of the inductor is ~5 times smaller than that of the varactor, the Q of the overall LC tank is limited by the inductor. The phase noise of a VCO in $1/f^2$ region (refer to Figure 6-20) can be approximated by Leeson's formula [Lee66], as follows:

$$L(\Delta\omega) = 10 \cdot \log\left(\frac{2FkT(Q_L^2 r_s)}{V^2} \cdot \left[1 + \left(\frac{\omega_o}{2Q_L\Delta\omega}\right)^2\right]\right) , \qquad (6.6)$$

where F is the noise factor of the amplifier, k is Boltzmann's constant, T is the temperature, V is the voltage across the tank, Q_L is the Q of $L_{1,2}$, r_s is the series resistance of the inductor, and $\Delta\omega$ is the frequency offset from the carrier. Assuming that the last term in the equation is much greater than 1, and all other parameters except r_s in the equation are constant, a 50% Q degradation increases the phase noise by ~3 dB (10 log(2)), which is

significant. Thus, doubling the thicknesses of metals 5 and 6 should improve the phase noise to -108 and -116 dBc/Hz at 1-MHz and 3-MHz offsets, respectively. The power consumption should also decrease, since the voltage across the tank would remain approximately constant while the effective resistance of the tank (Q^2r_s) would increase. This explains why, to overcome the lower Q, the current level was increased, explaining the added power consumption listed in Table 6-3.

Finally, to understand the competitiveness of this VCO result with previously published results, the phase noise can be scaled to a 5-GHz regime. Thus, for a given inductor Q, the 15-GHz VCO would correspond to a 5-GHz VCO achieving a phase noise of -114.5 dBc/Hz at a 1-MHz offset. This result is ~2.5 dB less than that achieved in [Hun00c] at 5.35-GHz. However, if thicker metal is used for the inductors, the scaled result would then be comparable to [Hun00c], with a benefit of reduced power consumption.

6.6.3 Power Amplifier

The PA consists of 2 stages of inductively-loaded common-source amplifiers. Unlike the transistors in the VCO core, whose output noise is directly injected into the LC tanks, the transistor noise in the PA does not significantly degrade the VCO phase-noise performance. Also, because the transistors are turned on only half of the time, the effective output noise becomes even lower. Hence, NMOS transistors with larger current-per-unit-channel-width are used.

The first class-A stage serves as a pre-amplifier for the final power amplifier stage. The transistor widths of stage 1 are only 2/3 of that of M_1 in the VCO core, to avoid significantly loading the VCO output. At the tuned frequency, the single-sided output has an amplitude approximately equal to the supply voltage, with an offset voltage of $V_{dd,PA}$. The

second stage acts as a class-E amplifier without a bandpass filter (traditionally used to select the fundamental), and is tuned together with the antenna impedance. Hence, as the amplifier switches, both the fundamental and higher-order harmonics are transmitted. The size of the transistors in stage 2 is 3 times larger than that of the first stage. Due to the thin gate oxide and, thus, low gate-oxide breakdown voltage, the maximum output power is designed to be ~12 dBm (the voltage amplitude of the differential output is 2 V and the real part of the antenna impedance is ~125 Ω). The power efficiency is ~60%. The output power can be simply controlled by the supply voltage. Figure 6-22 shows a simulated differential output waveform across the antenna. The output waveform is not sinusoidal at the zero-crossing point due to the passing of higher-order harmonics in the PA, introducing distortion to the signal.

Figure 6-23(a) shows the measured small-signal S-parameters for a differential PA (referenced to 100 Ω). The input of this stand-alone PA had 50-Ω resistors to ground at each input node. To obtain the measurement, baluns are placed at the input and output of the PA to transform the unbalanced signals from the network analyzer to balanced signals

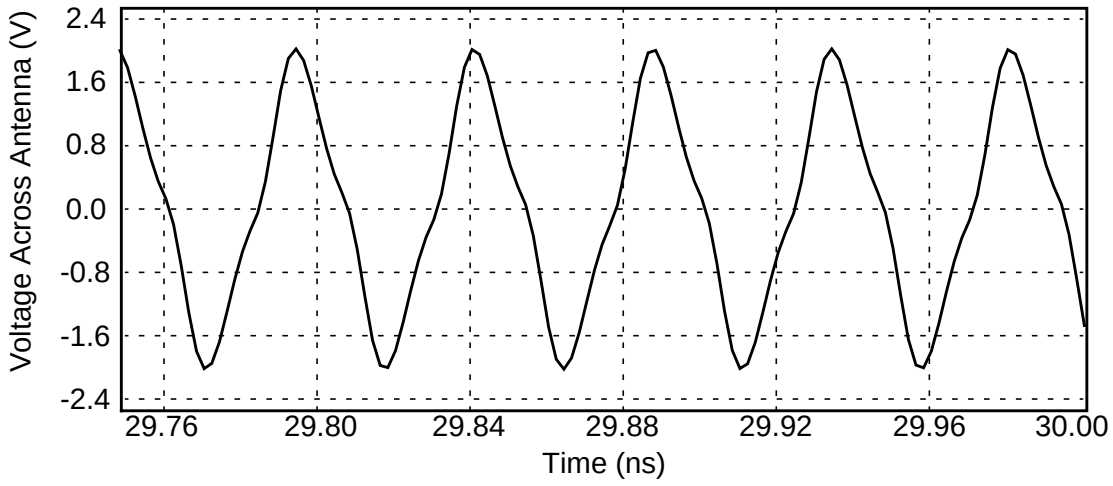


Figure 6-22 A simulated output waveform across the antenna from the PA.

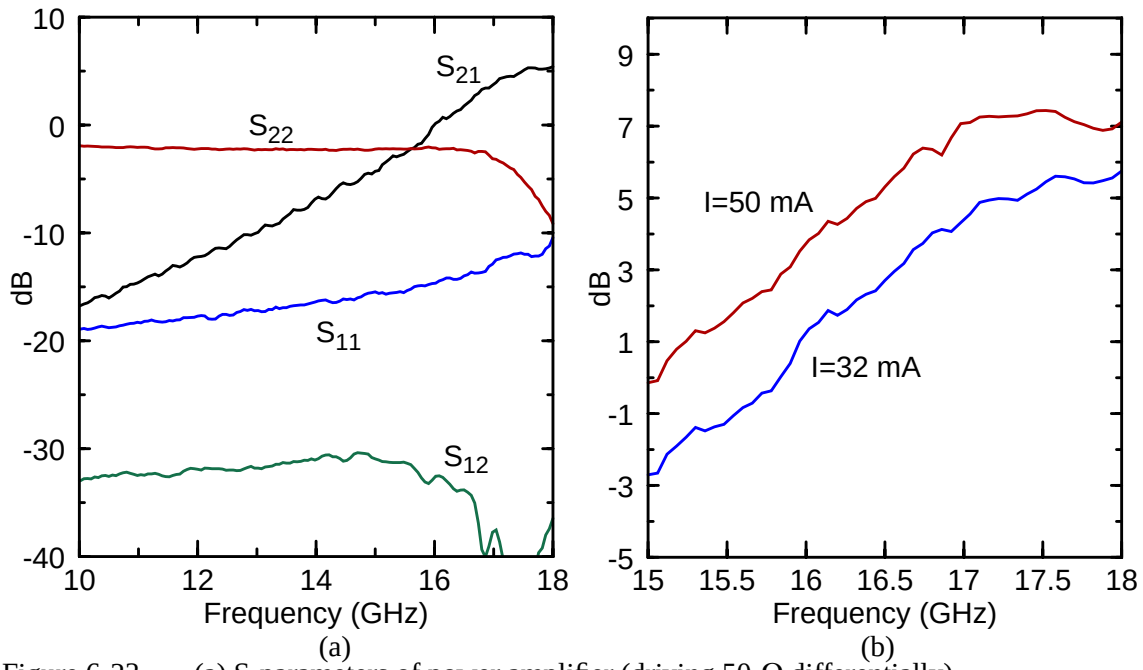


Figure 6-23 (a) S-parameters of power amplifier (driving 50-Ω differentially).
(b) Operating power gain of the PA when connected to a zigzag antenna.

for the PA. The frequency range of the baluns is limited to 18 GHz; thus, the measurement is also limited to this frequency range. The PA demonstrates an $|S_{21}|^2$ of 5.4 dB at 18 GHz, while consuming 41 mW from a 1.3-V supply. The S-parameters are obtained when driving a 100-Ω load. However, since the antenna impedance is not equal to 100 Ω and has a reactive component, the gain and resonant frequency for the PA driving the antenna are different than that from the S-parameter measurements. The operating power gain, plotted in Figure 6-23(b), is the ratio between the power delivered to the antenna and the power delivered to the input of the PA. The results show that the PA has a 6-dB operating power gain at 18 GHz. Because the peak gain frequency of the PA is de-tuned, the operating power gain at 15 GHz is less than one. Since the clock distribution system operates at 15 GHz, the PA is actually attenuating the signal from the VCO. If the power consumption of the PA is increased to 75 mW, the operating power gain at 15-GHz can be increased to 0 dB. Finally, the power delivered to the transmitting antenna is obtained from the

Table 6-3 Summary of measured characteristics for 0.18-µm CMOS VCO and PA

VCO	Expected	Measured	PA	Expected	Measured
Frequency Range	20-21.6 GHz	14.3-15 GHz	f_o	21 GHz	18 GHz
Power Consumption	3 mW	7.2 mW	Power Consumption	24 mW (V_{dd}=0.9V)	41 mW (V_{dd}=1.3V)
Phase Noise @ 1MHz	-	-105 dBc/Hz	Output Power to Antenna	+ 12 dBm	-13.2 dBm
Phase Noise @ 3MHz	-	-113 dBc/Hz	Operating Power Gain (f_o)	20 dB	6 dB

measurement of the full transmitter with an integrated antenna (discussed in the next section), revealing an available power of -13.2 dBm at 1.3 V to the antenna at 15 GHz.

Table 6-3 shows a comparison between the expected and measured PA results. As can be seen, the power gain of the amplifier is less than expected and the resonant frequency has been reduced. Decreasing the inductor Q by half should reduce the small-signal PA gain by approximately 7 dB. The first 6 dB comes from the pre-amplifier stage, whose output is a parallel resonant circuit composed of $L_{3,5}$ and shunt capacitances. Thus, the load impedance at resonance is proportional to the Q of $L_{3,5}$. Another 1-dB degradation comes from the second stage, where its output is loaded by the antenna. However, 7 dB of the gain reduction is still unaccounted for. Finally, the reduction in resonant frequency is due to increased transistor capacitances.

6.6.4 Clock Transmitter with Integrated Antenna

Referring back to Figure 6-17, the clock transmitter consists of a VCO connected to a PA, which then drives the transmitting antenna. Operation of the clock transmitter is demonstrated by on-chip generation of a global clock signal and reception of this signal

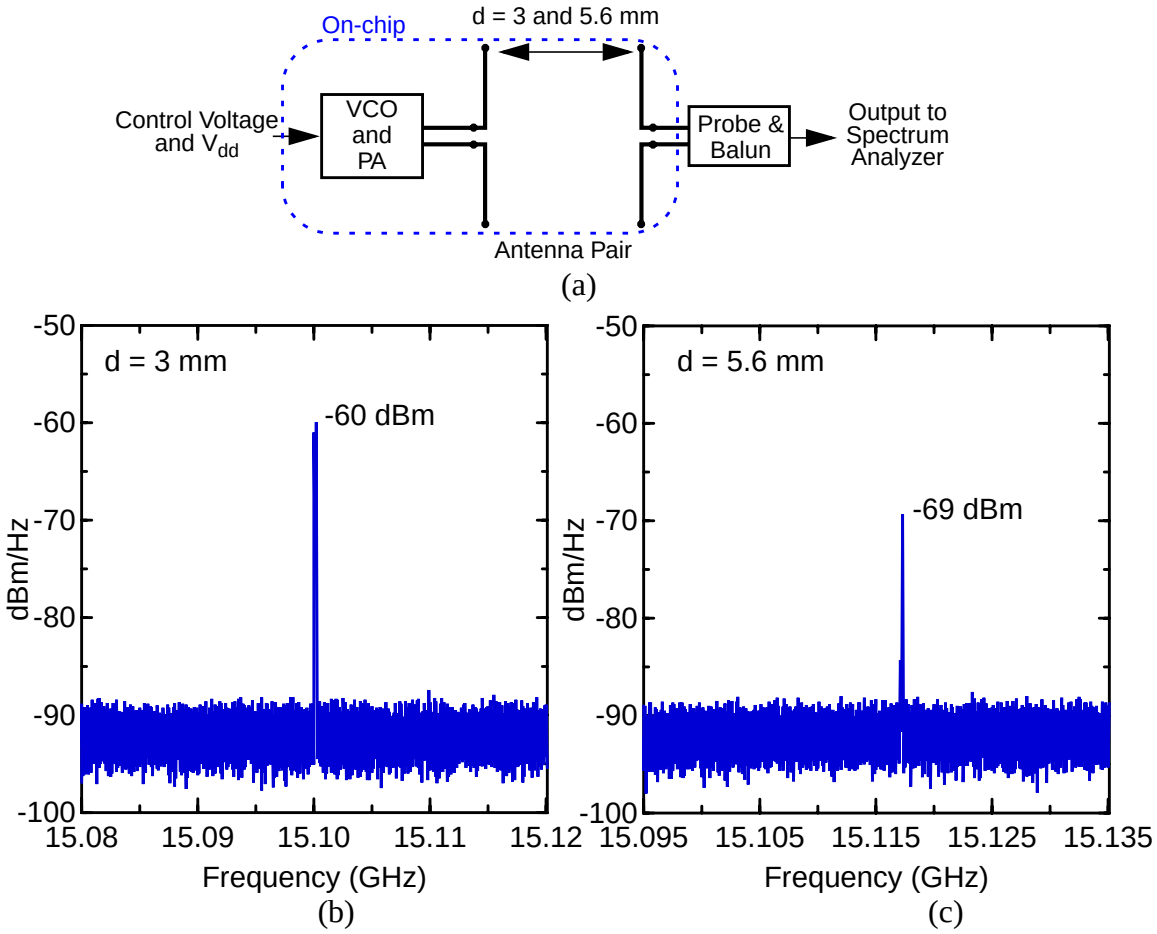


Figure 6-24 (a) Measurement setup used to characterize wireless clock transmitter. (b) & (c) Output spectra from receiving antenna detected from clock transmitter across a 3- & 5.6-mm distance.

using receiving antennas. Figure 6-24(a) shows a block diagram of the measurement setup used to test the clock transmitter. The DC control and supply voltages were supplied to a transmitter driving a zigzag dipole antenna. The output spectrum was then obtained by probing receiving antennas located at 3-mm and 5.6-mm separations from the transmitting antenna. Figures 6-24(b) and (c) show the resultant output spectra measured at 3-mm and 5.6-mm distances, respectively, having peak output power levels of -60 and -69 dBm at ~15 GHz. The transmitter consumes ~48 mW of power. Thus, an on-chip clock transmitter with an integrated antenna is demonstrated for the first time.

While this first on-chip wireless transmitter demonstration is significant, the received power level is very low. To understand this, the power delivered to the zigzag transmitting antenna by the PA is obtained using the measured G_a for the 6.7-mm antenna separation and calculating the mismatch loss in the system. At 15 GHz, the mismatch loss at the PA/antenna interface is 2.5 dB and the mismatch loss at the antenna/spectrum analyzer interface is 0.25 dB. These numbers are obtained using (5.3). Referring to Figure 6-13(a), the antenna transmission gain is -53 dB for a 6.7-mm separation.While this is not the measured gain for a 5.6-mm separation, it is within the deviation expected from varying metal interference structures, which is 5-10 dB, as demonstrated in Figure 6-14(b). Therefore, with an antenna transmission gain of -53 dB, the extracted power available from the PA is -13.25 dBm (-69 + 0.25 + 53 + 2.5), while the power delivered to the zigzag antenna is -15.75 dBm (-13.25 - 2.5).

The PA was originally designed to deliver +12 dBm to the antenna; thus, there is a 28-dB difference between the expected and measured results. Referring back to section 6.6.3, the reduction in inductor Q due to thin metals 5 and 6 accounts for 7 dB of the PA gain reduction. Second, operating the PA at 15 GHz, as opposed to at its resonant frequency (18 GHz), accounts for another 8.5 dB. Third, the dc-bias level provided by the VCO at the input of the PA is less than that used to characterize the stand-alone PA. This reduced bias point is due to the VCO core current being increased to overcome the Q reduction. Thus, the transconductance of the PA is decreased, resulting in another ~7.5-dB degradation. Taking all of these effects into account, the expected power delivered by the PA should be -11 dBm. This is close to the measured PA's available power of -13.25 dBm, which assumes that the PA and the antenna are conjugately matched, as was the case in the

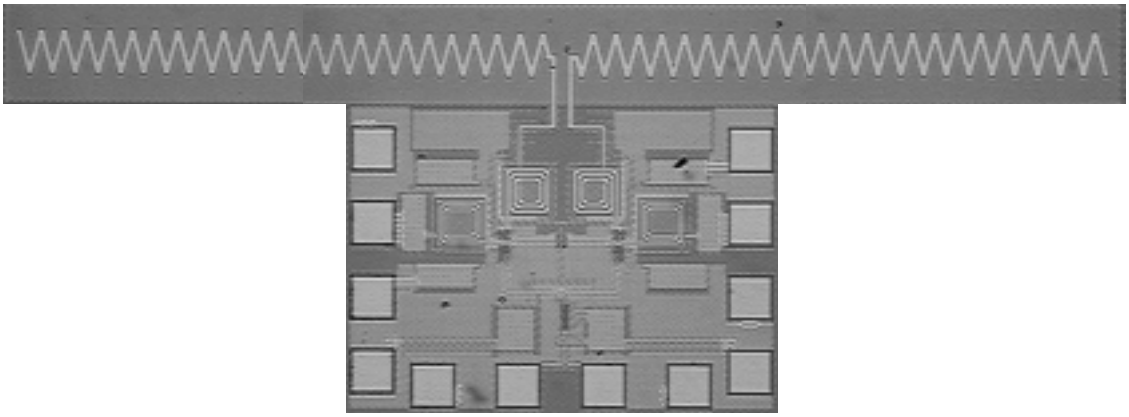


Figure 6-25 Die photograph of 0.18-μm clock receiver with zigzag dipole antenna.

simulations. In summary, although operation of the wireless transmitter has been demonstrated, the power that the transmitter can provide to the receivers through the antenna pair is very low and as will be shown in the next section, is below that which the receiver can detect. As can be seen, the PA appears to be the weakest link in the transmitter, and requires circuit optimization.

6.6.5 Single Clock Receiver with Integrated Antenna

Figure 6-25 shows a die photograph of the 0.18-μm clock receiver with an integrated zigzag dipole antenna. The size of the receiver, including the antenna, is 0.66x2 mm^2, while the active area is 0.37x0.58 mm^2. The receiver consists of a zigzag dipole antenna, a differential LNA with source-follower buffers, an 8:1 frequency divider, and output buffers. The performance of the 0.18-μm LNA and source-followers was presented in Chapter 3, while the divider performance was presented in Chapter 4. A summary of the results is shown in Table 6-4, for easy reference. To decrease the minimum detectable signal of the receiver, the peak LNA/buffer gain should coincide with the self-resonance of the frequency divider. To achieve this, the supply voltage of the frequency divider was

Table 6-4 Summary of measured characteristics for 0.18-μm CMOS LNA and divider

LNA and SF Buffer	Expected	Measured	Frequency Divider	Expected	Measured
f_o	21 GHz	14.4 GHz	Division Ratio	8:1	
Gain	27 dB	21 dB	f_{max} (V_{dd}=1.5V) (V_{dd}=2.1V)	35 GHz 42 GHz	15.8 GHz 20.4 GHz
NF	2.94 dB	8 dB	f_{iSO} (V_{dd}=1.5V) (V_{dd}=2.1V)	28 GHz 34 GHz	9.15 GHz 14.2 GHz
Power	11.2 mW	28 mW	Power (V_{dd}=1.5V) (V_{dd}=2.1V)	6 mW 18.5 mW	4.5 mW 12.2 mW

increased from 1.5 to 2.1 V, increasing f_{iSO} from 9.2 to 14.2 GHz. Operation of the clock receiver is demonstrated by transmission of a global clock signal across the chip, detection of this signal, and generation of a local clock signal by a single clock receiver.

The same measurement setup shown in Figure 6-9(a), and again in Figure 6-26(a), was used to test the clock receiver. The input signal is generated off-chip and externally amplified. This signal is then transformed into a balanced signal and injected into the transmitting antenna on-chip. The output of the receiver located across the chip is then probed and examined using an oscilloscope. Two clock receivers (Rx1 and Rx3 from Figure 6-10) were tested, having antenna separations of 3.2- and 5.6-mm, respectively. Figure 6-26(b) shows plots of the input voltage to the transmitting antenna and the output voltage for the wireless clock receiver, for a 5.6-mm transmission distance (Rx3), demonstrating operation of the clock receiver with integrated antenna. The input global clock frequency is 15 GHz, and the output local clock frequency is 1.875 GHz (15 GHz divided by 8). The minimum power level needed at the transmitter for the clock receiver to lock to the input signal is 20.33 dBm. Note that the input signal plotted in Figure 6-26(b) is taken before the

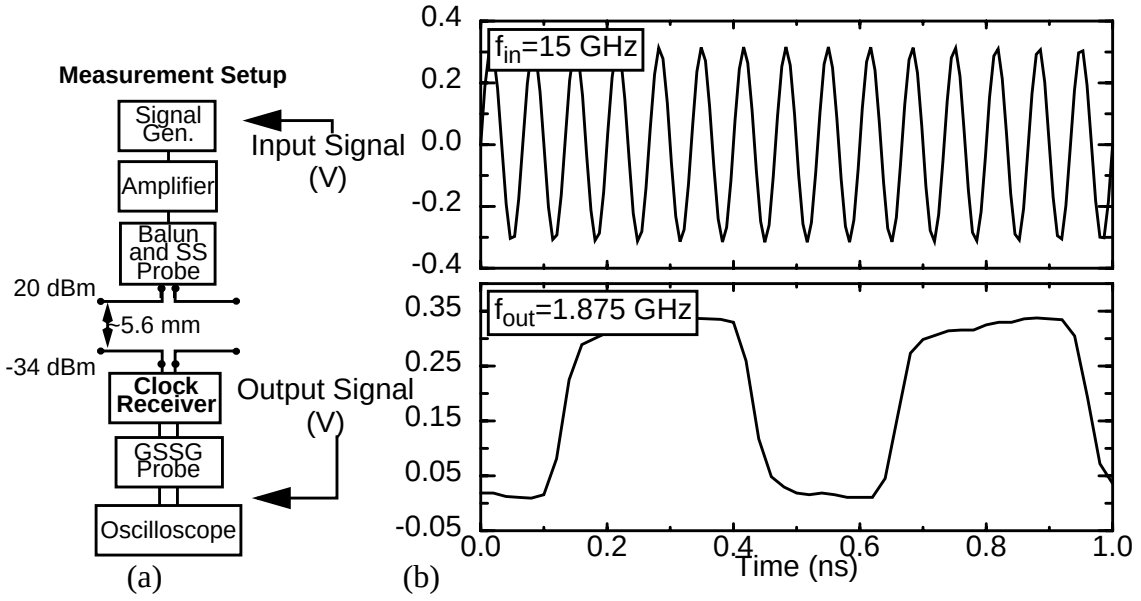


Figure 6-26 (a) Measurement setup used to characterize wireless clock receiver.
(b) Input and output wave-forms for clock receiver, demonstrating operation of receiver for 5.6-mm separation at 15 GHz.

external amplifier. The reduced voltage swing at the output results from driving a 50-Ω load. The total power consumption for the receiver is 40 mW. Inferring from the measured zigzag-zigzag antenna pair transmission gain (~ -53 dB) and accounting for mismatch loss in the system, the power delivered to the input of the receiver is -34.3 dBm. As expected, for the 3.2-mm separation, the input power level to the transmitting antenna can be 10 dB lower, since the antenna transmission gain is 10 dB higher.

6.6.6 Simultaneous Transmitter and Receiver Operation

By comparing the results from both the transmitter and receiver circuits with integrated antennas, it can be seen that simultaneous operation of these two circuits (i.e., integrated transmitter communicating across the chip to integrated receiver) is currently not possible. The input power level for the receiver is -34.3 dBm, while the power received from the transmitter is -60 and -69 dBm for half-chip and full-chip transmission,

respectively. Thus, there is a 25.7-dB and 34.7-dB deficit in “system gain” for achieving a fully integrated half- and full-chip wireless clock distribution system, respectively. A primary reason for this deficit is the reduced thickness of metals 5 and 6. As has been shown, the effect of lower than expected inductor Q and reduced operation frequency has reduced the overall system gain. First, the 50% Q degradation reduced the PA gain by at least 14.5 dB (Q and g_m effect) and has reduced the LNA gain by approximately 6 dB. Second, referring to Figure 6-13(a), operating the antennas at 15 GHz, as opposed to at 21 GHz, results in approximately 8 dB less transmission gain for the full-chip transmission distance. Also, the mismatch in the VCO frequency range and peak gain frequency for the PA led to another 8.5-dB degradation of the system gain (the PA appears to currently be a sensitive spot in the system). Therefore, a 37-dB difference can be accounted for, indicating that the fully-integrated system would have worked if the copper thickness was doubled and the operating frequency had been above 18 GHz. As it is, by just doubling the metal thickness of metal 5 and 6 layers, the system gain will increase by approximately 20.5 dB, which should be enough to allow operation of the fully-integrated half-chip distribution system.

As mentioned earlier, these designs were implemented as part of the SRC Copper Design Challenge. Due to circuit fabrication problems at UMC and the thinning of the top-layer metals, the masks are being regenerated and another run is forthcoming. With this new run, it is expected that all of the circuit performances will dramatically improve and that simultaneous operation of a clock receiver and transmitter will be achieved.

6.7 Double-Receiver Wireless Interconnect

A critical test for the wireless clock distribution system is to demonstrate two clock receivers operating simultaneously and synchronously from the same transmitted

global clock signal. From this test, the clock skew and jitter can be evaluated. Also, this will demonstrate a larger and more realistic portion of the system, in that time-of-flight delays, amplitude mismatch, and process variation will all be present.

The receivers used for the double-receiver test are Rx2 and Rx4, located in the upper and lower right-hand corners of the 0.18-μm UMC testchip, as shown in Figure 6-10. These receivers contain programmable dividers, allowing the startup phase of the circuit to be adjusted in 45^o increments, as presented in section 4.6. This programming is used to tune out any time-invariant delay mismatch between the receivers, limiting the clock skew to under 6.25% for an 8:1 divider. The transmitting antennas used for the double-receiver test are Z_{6b} and Z_{6c}, positioned on the left-hand side of the chip. Antenna Z_{6b} is located 5.95 mm from both Rx2 and Rx4, while Z_{6c} is located 6.8 mm from Rx2 and 5.6 mm from Rx4.

6.7.1 Measurement Setup

The double-receiver measurement is illustrated in Figure 6-27. The input global clock signal (GCLK) is generated off-chip and externally amplified. Before the amplifier, GCLK is split, allowing it to be measured with an oscilloscope. The GCLK signal is then transformed into a balanced signal and injected into the transmitting antenna, Z_{6b} or Z_{6c}. The receivers, Rx2 and Rx4, are probed and their outputs are examined using an HP 54120B digitizing oscilloscope mainframe and HP 54121A four-channel test set. Since each receiver produces out-of-phase local clock signals, the in-phase signals from Rx2 and Rx4 were measured, while the out-of-phase signal from Rx4 was used as the trigger for the oscilloscope. The out-of-phase signal from Rx2 was terminated with a 50-Ω load.

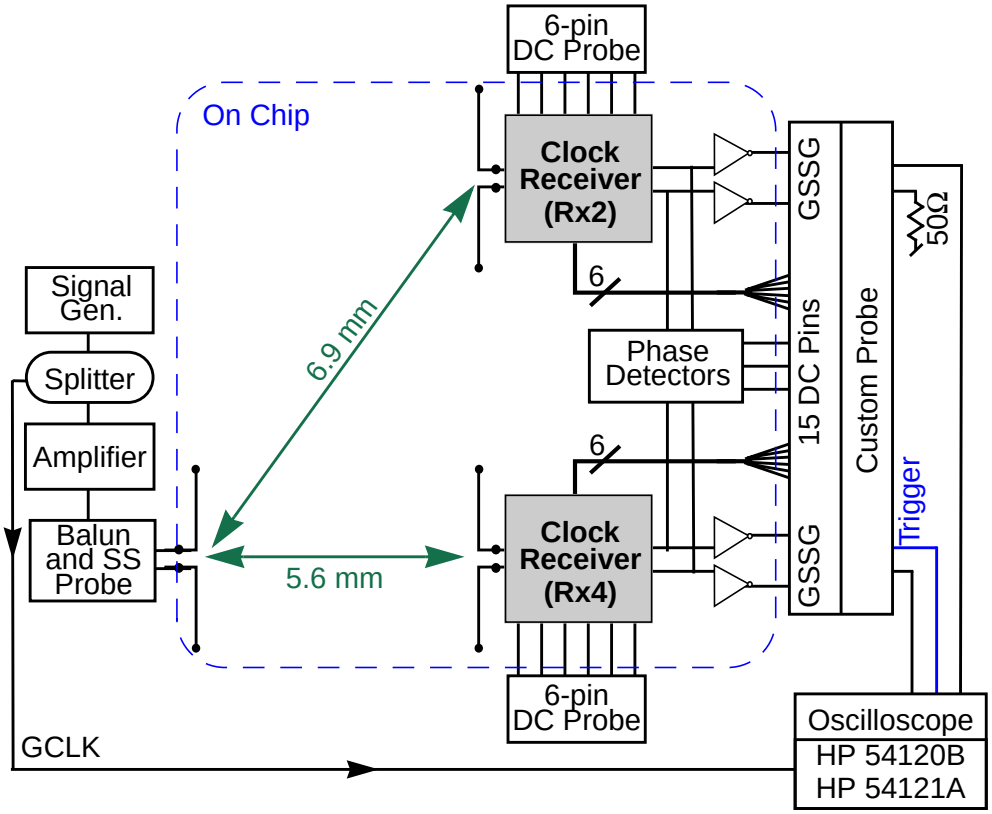


Figure 6-27 Diagram of measurement setup developed for double-receiver interconnect.

Measuring the clock skew between two clock receivers using wafer probing would require matching the delay through the external measurement system, such that the measured clock skew is due only to the skew in the circuits themselves. Since this is difficult at ~2 GHz, the clock skew is detected on chip using a phase detector (PD). The PD converts on-chip skew to voltage, as presented in Chapter 4, section 4.6.5. The PD is symmetric with respect to both input signals, preventing a systematic skew or phase difference from arising in the PD itself. As shown in Figure 4-26(b), the output voltage response from the PD is approximately linear versus input skew, and is symmetric with respect to the y-axis.

A customized probe was required to measure the two receivers and the phase detector output simultaneously. Since each clock receiver has probes on three sides, the outputs from two sides of each receiver were routed such that one probe could be used in

place of four original probes. Therefore, a 23-pin probe was required (obtained from GGB Industries), having a ground-signal-signal-ground ac probe for each receiver, as well as 15 dc pins to bias each receiver and measure the phase detector. Bypass capacitors were placed on each dc supply pin to filter low frequency noise. Due to the pitch and number of probes, these surface-mount capacitors were placed by GGB during probe manufacture.

6.7.2 Demonstration of Double-Receiver Interconnect

First, the double-receiver interconnect was measured using Z_{6b} as the transmitting antenna. This antenna is located 5.95 mm from each clock receiver. For this measurement, the UMC testchip was mounted on a glass slide and placed on a 1-cm thick wood slab (refer to Figure 6-4), which rested on the metal chuck of the probe station. Figure 6-28 shows the measured results for the double-receiver wireless interconnect. The input frequency is 15 GHz and the output frequencies for both clock receivers are 1.875 GHz. The input power available to the transmitting antenna is set to 20.7 dBm.

As can be seen, this result demonstrates two receivers operating simultaneously. From the figure, the two clock signals appear to have very low skew. However, this can be misleading, because these waveforms were obtained through the external cables in the measurement system. Thus, there is skew induced by mismatches between each cable and its connectors. The extracted on-chip skew for this case obtained with the phase detector will be presented in the next section. To obtain the power delivered to each receiver, the antenna transducer gain was measured for each antenna pair with a wood dielectric layer beneath the chip. The measured antenna transducer gains at 15 GHz are -60 dB for both antenna pairs $Z_{6b\text{-}6a}$ and $Z_{6b\text{-}6c}$. From the antenna impedance, the input impedance of the

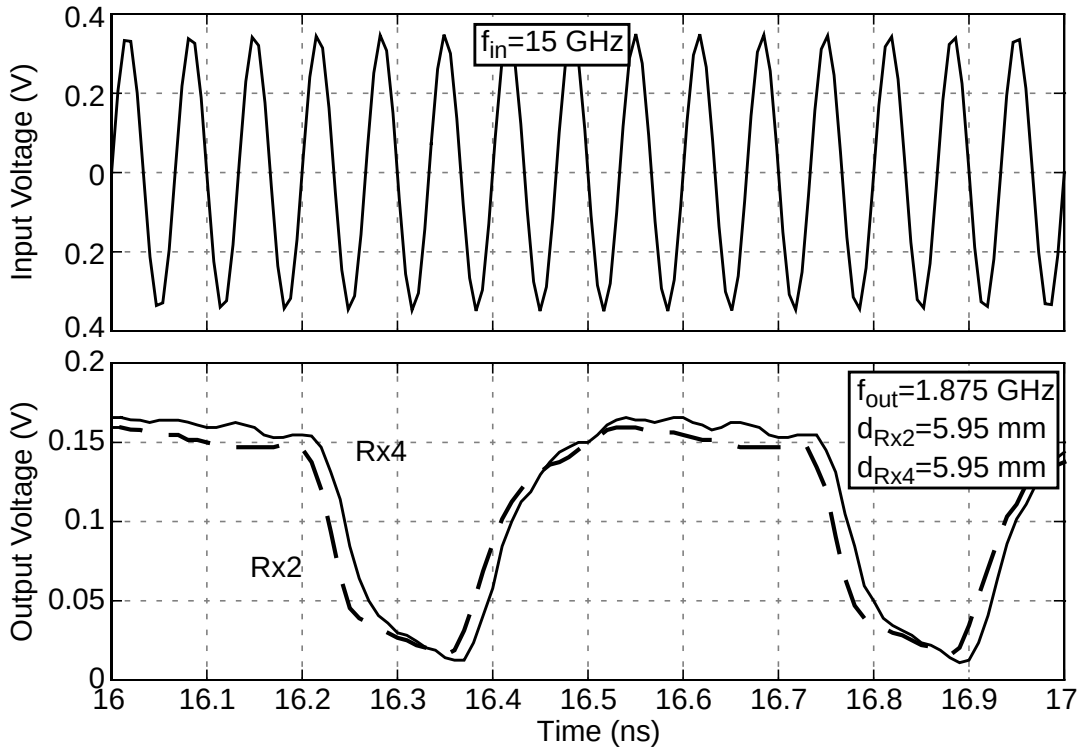


Figure 6-28 Measured input and output waveforms of double-receiver interconnect using Z_{6b} as the transmitting antenna, with a wood as the back dielectric. Input frequency is 15 GHz; output frequencies are 1.875 GHz; distances are 5.95 mm, each.

receiver, and the impedance of the input balun, the mismatch loss in the system is calculated to be 0.6 dB. With a 20.7-dBm available input power, the power delivered to each receiver is -39.9 dBm, corresponding to the minimum detectable signal for the receiver.

The second double-receiver interconnect was demonstrated using Z_{6c} as the transmitting antenna. This case is of particular interest since Z_{6c} is located 6.8 mm from Rx2 and 5.6 mm from Rx4. At 15 GHz, the wavelength of the transmitted signal is 10.1 mm in silicon-dioxide and 5.8 mm in silicon. Therefore, a time-of-flight delay mismatch between 8-12 ps is present in the system, where the actual value depends on the effective dielectric constant for this multi-path medium. Additionally, the transducer gains for each antenna pair are not equal; thus, there will be a skew due to amplitude mismatch at the input of the divider. These skews will be tuned out using the programmable divider.

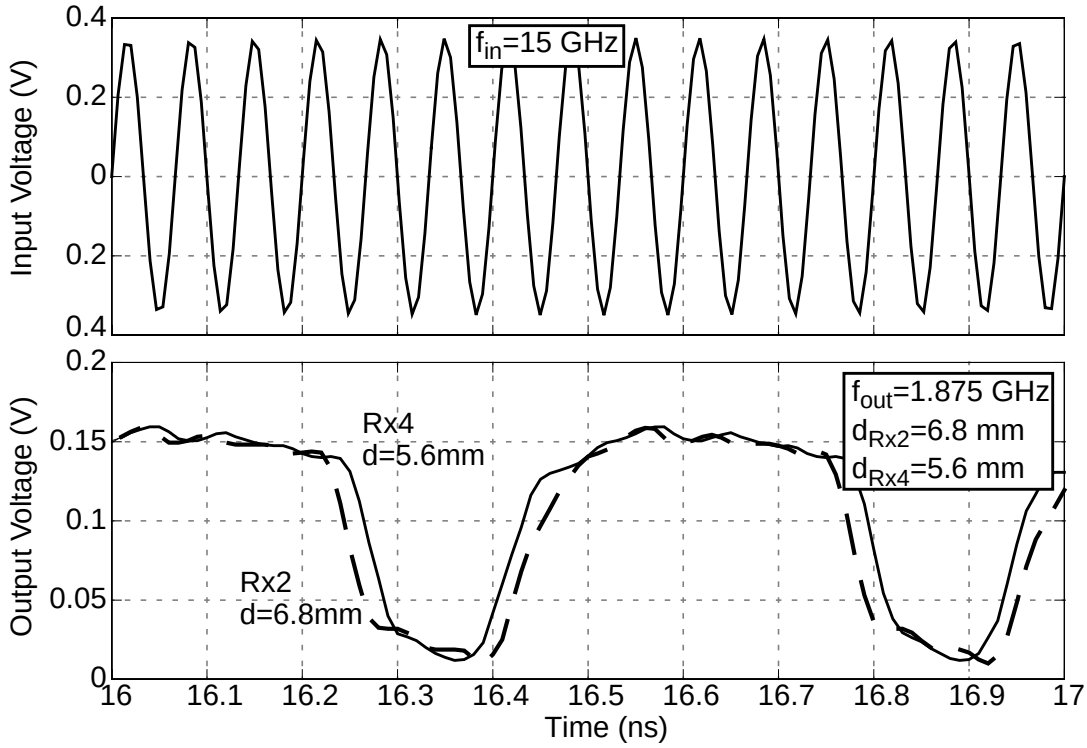


Figure 6-29 Measured input and output waveforms of double-receiver interconnect using Z_{6c} as the transmitting antenna, with a AlNi as the back dielectric. Input frequency is 15 GHz; output frequencies are 1.875 GHz; distances are 6.8 mm for Rx4 and 5.6 mm for Rx2. Time-of-flight delay mismatch and amplitude mismatch are present.

For this second measurement, the UMC testchip was mounted on a glass slide and placed on a 0.76-mm thick slab of aluminum nitride (AlN). This thickness was chosen based on the results presented in [Guo01]. Recall that AlN has a high thermal conductivity (approximately the same as silicon), while still being a good dielectric (κ_{AlN}=8.5). Thus, it is a suitable medium for the backside dielectric layer which will be connected to the heat-sink. Figure 6-29 shows the measured waveforms for the double-receiver interconnect with Z_{6c} as the transmitting antenna. Once again, the input frequency is 15 GHz and the output frequencies are 1.875 GHz, demonstrating two receivers operating simultaneously. The clock skew for this case will be presented in the following section, however, by inspection, the skew appears to be similar to the result shown in Figure 6-28.

The measured transducer gains for the antennas on the AlN substrate at 15 GHz are -54.1 dB for antenna pair $Z_{6c\text{-}6a}$ (distance = 6.9 mm) and -60.1 dB for antenna pair $Z_{6c\text{-}6c}$ (distance = 5.6 mm). Interestingly, the gain for the diagonal pair, $Z_{6c\text{-}6a}$, is larger, even though the distance is greater. This seems to indicate that the signal degradation due to interference structures is greater for antenna pair $Z_{6c\text{-}6c}$. With a 20.7-dBm available input power to the transmitting antenna, and a 0.6-dB mismatch loss, the power delivered to each receiver is as follows: -34 dBm for Rx2 and -40 dBm for Rx4. The 6-dB difference in input power levels can result in as much as 2.1% of clock skew, according to section 5.4, equation (5.17) (i.e., skew = $\frac{1}{16\pi}\cos^{-1}\{10^{-6/20}\}$). Thus, at least a total of between 3.6-4.4% of systematic clock skew due to time-of-flight delay mismatch and amplitude mismatch should be present in this measurement.

6.7.3 Measured Skew Between Two Clock Receivers

The skew between the two receivers (for the case with Z_{6b} as the transmitting antenna) was extrapolated from the response of the phase detector when the start-up states of the dividers were varied across their 8 possible values. Since the skew induced by the measurement system will be constant at a single frequency, the output of the phase detector can be compared to the skew measured with the oscilloscope. This results in a voltage-versus-skew response for the phase detector which should be maximum at the point of zero skew between the two input signals, and which should be similar to the response shown in Figure 4-26(b).

As discussed in Chapter 4, the programmable divider has a state-dependent initialization failure which causes the divider to initialize to any of the 8 possible states for a given input desired state. The programmed state depends on the state of the divider when

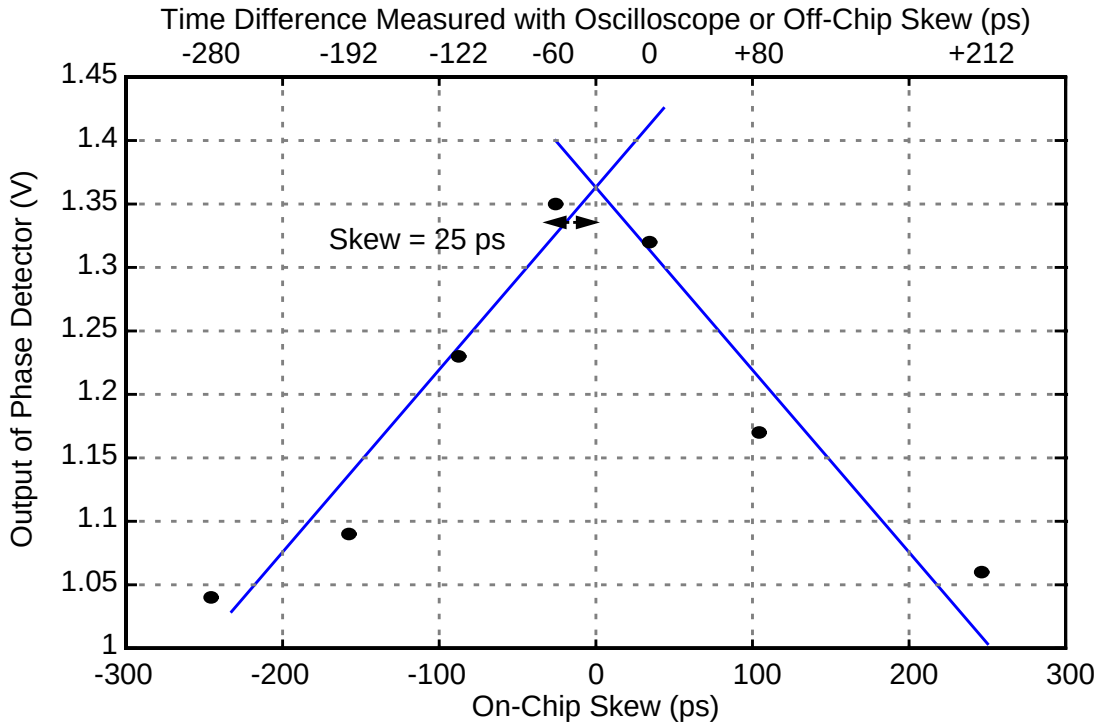


Figure 6-30 Measured output of phase detector versus time difference (skew) measured between waveforms from Rx2 and Rx4 using oscilloscope. Lines with equal and opposite slopes are fit to both the positive and negative portions of the curve, where the lines intersect at the point of zero skew.

the initialization signal is engaged. Even with this failure, though, the divider will take on discretized states or phases; thus, the minimum adjusted skew can still be extracted.

Figure 6-30 shows the output voltage of the phase detector versus the skew between the two waveforms measured with the oscilloscope through the external measurement system. The top x-axis is for skew measured directly with the oscilloscope or off-chip skew, which would include skew added by the measurement system. Using these values, lines are fit (using Matlab) to both the increasing and decreasing portion of the voltage response. The slopes of these lines are set to be equal and opposite since the phase detector has a response which has even-order symmetry with regards to input skew. The phase detector was designed such that both inputs have identical loads, eliminating any systematic phase error. Under this assumption, the two lines in Figure 6-30 intersect at the

point of zero input skew. From this intersection, the skew added by the measurement system can be determined to be -35 ps. This then allows the on-chip skew to be determined by subtracting -35 ps from the measured off-chip skew, resulting in the second x-axis in Figure 6-30. Thus, the minimum on-chip skew is 25 ps, which is 4.7% of the local clock period. By adjusting the start-up states of the dividers, the skew can be reduced to under 5%, which is the requirement set for global clock distribution systems. This same skew extraction methodology has been applied to the case where Z_{6c} is used as the transmitting antenna, showing 20 ps of skew, or 3.75%. This is significant, since the measurement case has at least 3.6-4.4% of systematic skew due to time-of-flight delay mismatch and amplitude mismatch, in addition to process variation.

Unfortunately, the uncorrected or unprogrammed skew can not be determined from this measurement. This is due to the state-dependent initialization failure of the dividers. If the dividers initialize properly, then the uncorrected skew would be the skew measured when both dividers are initialized to the same state. However, since each divider currently initializes to a random state, it is impossible to know if the dividers are initialized to the same state, which would yield the uncorrected skew. The results do, however, show that programming the dividers can tune out systematic skew.

6.7.4 Measured Jitter of Clock Receivers

The jitter of these receivers has been measured using the setup already shown in Figure 6-27. To measure the peak-to-peak jitter, the triggered waveforms can be displayed with an infinite persistence. The jitter is measured off of the input 15-GHz signal rather than one of the 1.875-GHz output signals. This is because the trigger signal is also a 1.875-GHz clock signal which has its own jitter. Thus, measuring the jitter of the 15-GHz

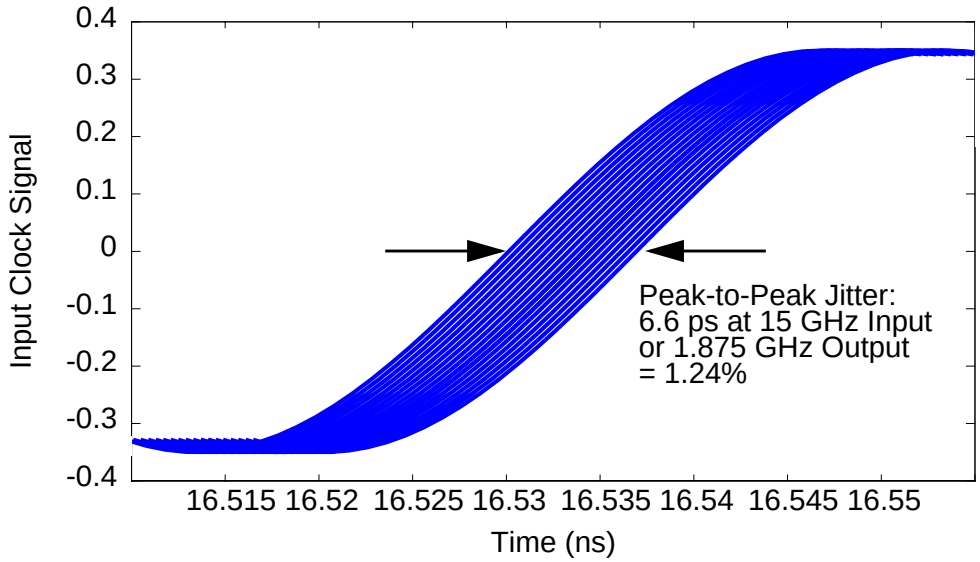


Figure 6-31 Illustration of the measured jitter of the wireless clock receiver. This jitter was measured off of the 15-GHz input signal, yielding the jitter of the 1.875-GHz output signal used as the trigger. The measured peak-to-peak jitter was 6.6 ps.

signal, which should have very small jitter or phase noise, yields the jitter of the triggered 1.875-GHz waveform. An *illustration* of the resultant plot with infinite persistence is shown in Figure 6-31. This is an illustration, rather than the real data, since a screen capture of the oscilloscope could not be obtained. The measured peak-to-peak jitter is 6.6 ps at 1.875 GHz, corresponding to 1.24% of the local clock period. This is under the system requirement of 3% peak-to-peak jitter. Note that this jitter is for a “quiet” system, meaning that the supply voltages are not being modified by digital circuits. In the literature, this is known as the quiet-supply jitter. In an operating microprocessor, the jitter will be increased, due to larger switching noise and noisy supplies.

The signal-to-noise ratio at the input of the divider can be determined using (5.35) and the measured jitter, and assuming that the jitter is dominated by input additive noise. Assuming that the RMS jitter is one-sixth of the peak-to-peak jitter (or 1.1 ps = 0.2%), then the SNR at the divider input is calculated to be 19.7 dB. This agrees remarkably well

with the SNR of 21.8 dB estimated using SPICE, which was presented in section 5.7 of Chapter 5. Since the system requirement for the SNR to obtain 0.5% RMS jitter is 12 dB, a 7.7-dB margin is present. However, this margin could of course be consumed (and perhaps exceeded) by the interference due to digital switching noise.

6.8 Summary

In this chapter, the implementation of on-chip wireless interconnects with integrated antennas has been presented. Two different test chips have been implemented--one in a 0.25-μm CMOS process and one in a 0.18-μm CMOS process. Measured antenna characteristics for both chips show that antenna gain increases with frequency where the antenna becomes electrically longer. Also, the presence of interference structures between the antennas can alter the gain by 5-10 dB. Loop antennas and antennas in direct contact with the substrate have been characterized, and show promising results for higher frequencies. Additionally, the phase versus frequency response for the antennas is linear indicating wave propagation, while the gain between two sets of pads is at least 15 dB less than that for the antennas. These two facts together show that the signal coupling is due to wave propagation, and that these waves are launched much more efficiently from the antennas than from just the pads. Finally, the impedance mismatch between the antenna and receiver degrades the minimum detectable signal of a clock receiver and hence, this impedance has to be accurately predicted *a priori*.

In the 0.25-μm test chip a clock receiver with integrated antenna was implemented. A 7.4-GHz global clock signal was successfully received over a 3.3-mm distance with interference structures located in between the antennas, and a 925-MHz local clock signal was generated. This result is the first demonstration of an on-chip wireless interconnect. Also, this result is the first to integrate antennas and CMOS circuitry on a single chip.

In a 0.18-μm copper technology, a 15-GHz wireless clock distribution system composed of integrated transmitters, receivers, and antennas has been implemented. A wireless transmitter with an integrated antenna generated and transmitted a 15-GHz global clock signal across a 5.6-mm test-chip, and this signal was detected using receiving antennas. The transmitter consisted of a VCO, PA, and antenna. Also, a wireless clock receiver with an integrated antenna detected a 15-GHz global clock signal supplied externally to an on-chip transmitting antenna located 5.6 mm away from the receiver, and generated a 1.875-GHz local clock signal. These results demonstrate wireless interconnection at 15 GHz for a 5.6-mm distance. This is the first known demonstration of an on-chip clock transmitter with an antenna and the second demonstration of a clock receiver. This result also virtually obsoleted the 0.25-μm result. Thus, by advancing the technology one generation, both the frequency and interconnection distance have been approximately doubled. This is quite significant, because it shows that the frequency of operation and the interconnection distance scale roughly with Moore's Law (using two data points).

Finally, a wireless interconnect composed of two clock receivers locked to the same global clock signal has been demonstrated at 15 GHz. The distances between the transmitting antenna and the two clock receiver are 5.95 mm each in one case, and 5.6 mm and 6.8 mm for the other case. The 6.8-mm interconnection distance is the longest to date. The results show that the two receivers are synchronized, having an output clock skew of 25 ps at 1.875 GHz (or 4.7%). The measured peak-to-peak clock jitter with quiet supplies is 6.6 ps at 1.875 GHz (or 1.2%). These results suggest that a wireless distribution system can meet the skew and jitter requirements for clock distribution systems. All of these results demonstrate the plausibility of an intra-chip wireless interconnect system containing integrated antennas and CMOS transmitter and receiver circuitry.

CHAPTER 7
FEASIBILITY OF WIRELESS CLOCK DISTRIBUTION SYSTEM

7.1 Overview

While wireless interconnects have been demonstrated, overall system feasibility has yet to be determined. One important feasibility issue is quantifying how much power a wireless clock distribution system will consume and evaluating if this consumption is within the budget allowed by the microprocessor. Another feasibility issue is evaluating the effects of process variation on operation of the wireless interconnect. Perhaps the most important feasibility issue is the clock skew and jitter of the system, since a clock distribution system inherently has to be synchronized, else the whole function of a global clock signal is compromised. This chapter estimates the worst-case clock skew and jitter that will be obtained and compares these estimations to the measured skew and jitter presented in Chapter 6. Also, the latency of the wireless interconnect is presented, along with how this latency should scale with technology generations. Two intangible feasibility issues are the area consumed by the transmitter and receivers, which has to be weighed against the top-level metallization being conserved, and the design verification of the system. Using these results, the current feasibility of the system is discussed. This is then followed by overall conclusions for wireless clock distribution and suggested future directions.

7.2 Power Consumption Analysis

Whenever circuits are optimized for the highest possible operating frequency, it is usually accompanied by an increase in the power dissipation. Since the wireless system

requires 16 or more clock receivers operating at 20 GHz or higher to be implemented on-chip, this added power dissipation by the receivers is a concern. To evaluate the impact these receivers have on the total power consumption of microprocessors, the power requirements for a wireless clock distribution system are estimated for the 0.1-μm generation, and then compared to those for conventional global clock distribution systems.

7.2.1 Power Consumption Comparison Methodology

The entire clock distribution system can be divided into a global system and a local system. The global distribution system is assumed to be the network which delivers the clock from its source (off-chip or on-chip) to various locations throughout the chip. The local distribution system is assumed to be that which takes the global clock, generates different clock phases as needed, and distributes these signals to all of the local circuits.

The power dissipation of the *global* distribution system can be modeled as dynamic, according to the following formula:

$$P_D = C_T V_{dd}^2 \cdot f , \tag{7.1}$$

where C_T is the total (equivalent) global capacitance being switched, including the capacitance of buffers, V_{dd} is the system supply voltage, and f is the clock frequency. To compare the power requirements between different types of global clock distribution systems, the system voltage and frequencies are assumed to be equal. Also, an equal capacitive load, representing the local clock generators or distribution system, is assumed for each type of global distribution system. Under these assumptions, the power dissipation can be converted to capacitances and these can be used to compare the power dissipation of different global distribution systems, similar to an approach taken in [Res98].

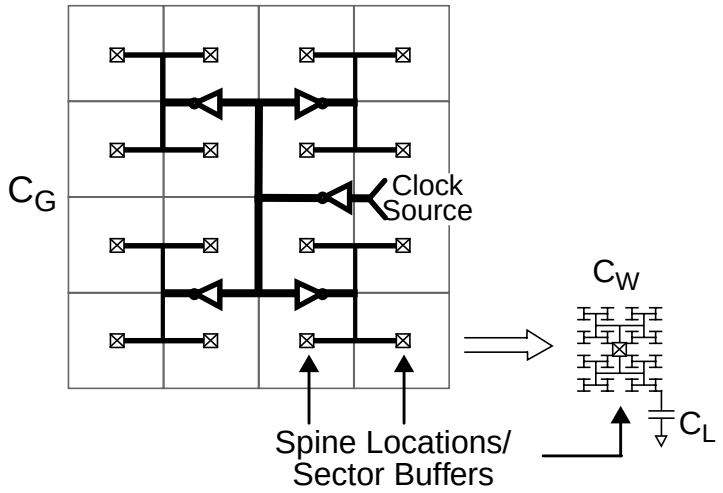


Figure 7-1 Illustration of total global clock capacitance.

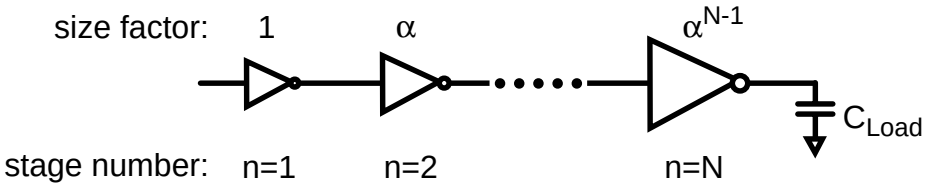


Figure 7-2 Schematic of tapered buffer used in global clock distribution. Each stage is α times as large as the previous buffer stage, resulting in minimum delay.

The total global capacitance can be allocated among three components, as follows: C_G, C_W, and C_L [Flo99b]. These components are illustrated in Figure 7-1. C_G is the equivalent capacitance of the highest level network which delivers the clock from its source to various sectors or spine locations distributed throughout the chip. C_G includes the total capacitance of the final driver stage (herein termed the sector buffer) plus any buffers leading up to the sector buffer. The multi-stage buffers, shown in Figure 7-2, are assumed to be tapered, where each buffer stage is α times as large as the previous buffer stage. It can be shown that this results in minimum delay through the buffer chain [Mea80]. The total capacitance of an N-stage buffer driving a capacitive load, C_{Load}, can be estimated as

$$C_{buffer} = (C_{Load}) \sum_{n=1}^{N} \left(\frac{1}{\alpha}\right)^n \Bigg|_{\alpha = e} \cong 0.57(C_{Load}). \quad (7.2)$$

A second component to C_T is C_W, which is the capacitance of the interconnecting wires for delivering the clock from the output of the sector buffers to the local distribution system. Finally, C_L is the load capacitance representing the input capacitance of the local clock generators.

The capacitances for the wireless system are based on measured results. The capacitances for the grid and H-tree systems are based on published 0.25-µm results [Res98, Gie97, Web97], which are then scaled to correspond to a 0.1-µm generation. The initial data for the total global capacitance for grid and H-tree systems are shown in Table 7-1. The scaling methodology used assumes that the number of sectors or spine locations scales with area. According to projections in [SIA99], the projected microprocessor areas are 300 and 622 mm^2 for 0.25- and 0.1-µm generations, respectively. Thus, C_G, C_W, and C_L each scale by a factor of 2.07. However, this scaling methodology does not account for all of the >10X increase in transistor density. To accommodate this increased load, either the drive capability in the local clock generators has to be increased or the grid and H-tree

Table 7-1 Total global capacitance for 0.25-µm technology

Capacitance (pF)	**Initial** 0.25-µm, Al, κ=4 2 V, 750 MHz	
	Grid	H-tree
C_G	1343	597
C_W	1400	95
C_L	600	600
$C_{Global} = C_G+C_W+C_L$	3343	1292
% Total Power	14.3	5.5

networks need to be adjusted. In this work, the former was chosen to keep the analysis straightforward. This results in shifting some power from the global distribution system to the local distribution system, resulting in an underestimation of the total global capacitance. However, since each clock distribution system drives an identical clock load, meaningful comparisons are still obtained.

Two cases are used in comparing these clock distribution systems for 0.1-μm generation microprocessors. Case 1 is for aluminum (Al) interconnects and conventional dielectrics; case 2 is for copper (Cu) interconnects and low-κ dielectrics. To obtain case 2, C_W and the components of C_G arising from wires were scaled by additional factors of 0.63 and 0.5, representing the decreased width of Cu-lines as compared to Al-lines for constant resistance lines, and the reduction in κ from 4 to 2, respectively.

7.2.2 Clock Distribution Systems

Grid-Based System. The grid-based system, shown in Figure 7-3(a) and based on DEC's 21264 [Gie97], consists of a global tree supplying the clock to different spine locations, and the capacitance of this network is C_G. These spines drive the clock grid, which has a capacitance C_W, from the four edges of the grid. The local clock generators then tap off of the grid. Due to the amount of wiring used to form the grid, C_W is large. Consequently, large sector buffers are needed, thereby increasing C_G.

H-Tree Based System. The H-tree system, shown in Figure 7-3(b) and based on IBM's S/390 [Web97], consists of a global tree supplying the clock to different sector buffer locations. Each buffer drives a balanced H-tree, which drives the local clock generators. C_W is smaller for the H-tree; therefore, a smaller sector buffer is required.

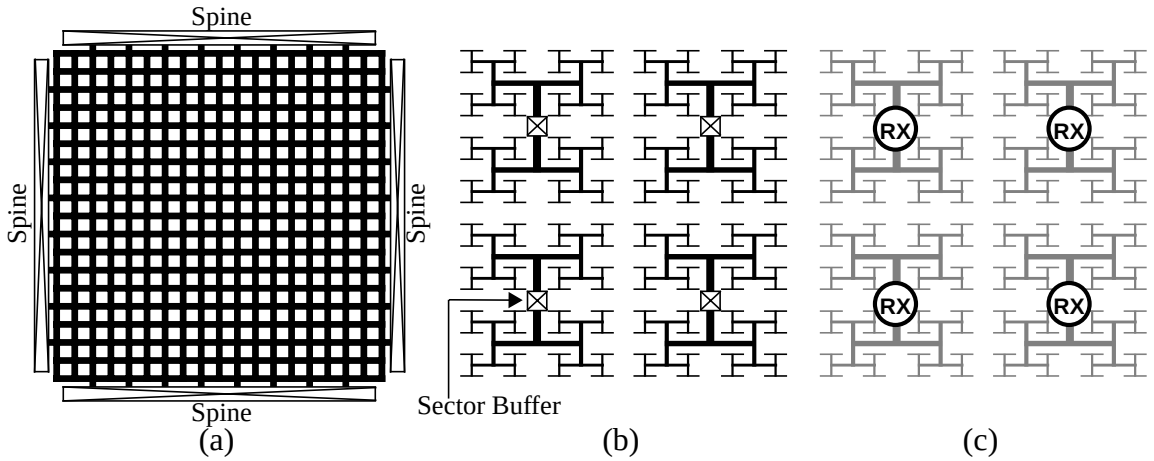


Figure 7-3 Illustration of *single quadrant* of global clock distribution systems for (a) grid, (b) H-tree, and (c) wireless.

Wireless System. The wireless system, shown in Figure 7-3(c), consists of a clock transmitter broadcasting a microwave signal to a grid of distributed receivers. Each receiver corresponds to a spine location and has a sector buffer at the output. Due to their low capacitance, balanced H-trees are used to distribute the signal from the receivers to the local clock generators. Thus, C_W for both the H-tree and wireless scheme is equal.

In a wireless clock distribution system, the long interconnects for delivering the clock from its source to spine/sector locations are not present, and the associated component of C_G is zero. However, since the wireless system contains components with static power dissipation, an equivalent global capacitance [Flo99b] representing this power dissipation is needed. The equivalent capacitance is defined as follows:

$$C_{Geq} = \frac{P_{TX} + N \cdot P_{RX}}{V^2 f}, \tag{7.3}$$

where P_{TX} and P_{RX} are the power consumptions of the transmitter and receiver, and N is the total number of receivers. Based on measured results for the 0.18-µm 15-GHz wireless interconnect, and assuming a 1.2-V supply, the transmitter consumes 38.4 mW while each

Table 7-2 Total global capacitance for 0.1-μm technology

Capacitance (pF)	**Case 1** 0.10-μm, Al, κ=4 1.2 V, 2 GHz			**Case 2** 0.10-μm, Cu, κ=2 1.2 V, 2 GHz		
	Grid	H-tree	Wireless	Grid	H-tree	Wireless
C_G	2523	1219	1129	1281	870	1064
C_W	2450	166	166	772	52	52
C_L	1242	1242	1242	1242	1242	1242
$C_{Global} = C_G+C_W+C_L$	6215	2627	2537	3295	2164	2358
% Total Power	11.2	4.7	4.6	5.9	3.9	4.2

receiver consumes 32 mW. The equivalent capacitance can then be used to make a comparison to the grid and H-tree systems.

7.2.3 Results and Conclusions for Power Consumption

Table 7-2 shows a breakdown of the global capacitive loading for the three distribution systems for cases 1 and 2. All capacitance units are in picofarads. The final row gives the power consumed by the global clock distribution systems as a percentage of total microprocessor power. This percentage represents the relative amount of power dissipated in the *global* system to drive a load of C_L. To obtain these numbers, the total power consumption projected in the ITRS is converted into an equivalent capacitance using (7.3) and then compared with C_{global}. For clarification, this percentage is not the relative amount of power dissipated in the entire clock system, which is estimated to be between 30 and 40% [Gie97]. This is because the percentage does not include the dissipation in the local clock distribution system, which will be much greater than the dissipation in the global system.

The results show that for both cases, the wireless system is comparable in performance to the H-tree system and better in performance than the grid-based system, in terms

of power dissipation. The results also show that technology developments such as Cu or low-κ will have the greatest positive impact on systems whose total equivalent capacitance is dominated by C_W, such as the grid. Finally, the results show that the power dissipated in the clock receivers, given by C_G, should be a small fraction (1.9%) of the total power dissipated in the microprocessor. These results show that power dissipation does not impose limitations for wireless clock distribution systems.

7.3 Process Variation

The wireless clock distribution system consists of multiple clock receivers distributed throughout the microprocessor. These receivers will have to be matched across the chip in terms of gain and phase so that the output local clock signals are synchronized. However, process variation and temperature gradients make this matching difficult; thus, there will be a nonzero clock skew due to process variation. The effects of process variation on a low noise amplifier, frequency divider, and clock receiver will be simulated in this section using Monte Carlo analyses, and the resultant local clock skew will be shown.

7.3.1 Simulation Methodology

Two ways process variation can be simulated are by using either corner models or Monte Carlo analyses. The corner models provide a worst-case variation that can be expected lot-to-lot, representing approximately a +/- 3σ variation. These models can basically be used to confirm circuit operation across all wafers. While this is important for the wireless clock distribution system, evaluating the variation within a *single die* is important as well. The within-die variation is simulated using Monte Carlo analyses in SPICE. With these analyses, select model parameters are defined by a probability density function

(PDF), and for each Monte Carlo iteration, SPICE randomly selects values for the parameters according to the PDFs (i.e., the values are more likely to be closer to the mean than to the mean +/- 3σ). This then provides statistical data for the simulated circuit, from which the single-die variation can be obtained.

The Monte Carlo model file was generated for the 0.25-μm CMOS circuits from TSMC. Every parameter that was varied in the corner models was replaced by a PDF, where the typical model parameters provided the mean value and the fast and slow corners provided the 6-σ variation. For example, in the corner models, the oxide thickness varies from a 5.5-nm thickness at the fast corner to a 6.1-nm thickness at the slow corner, having a typical value of 5.8 nm. Thus, the PDF of the oxide thickness is Gaussian[1] with a mean of 5.8 nm and a 3-σ variation of 0.3 nm. For the TSMC process, the following model parameters for both NMOS and PMOS were replaced with PDFs: oxide thickness, length and width variation, the threshold voltage at zero body-to-source voltage and low drain bias, the junction and sidewall capacitances, and the gate-overlap capacitances. In addition to these transistor parameters, the polysilicon sheet resistance was varied according to the process data (4.5 +/- 4 Ω/square). Finally, the resistance associated with the metal spiral-inductors was varied assuming a 3-σ variation of 10%.

1. In HSPICE, the parameter statement is either *variable = AGAUSS(mean, variation, sig),* or *GAUSS(mean, variation, sig)*. The mean and variation are specified, with *sig* being the number of standard deviations the variation represents. Here, AGAUSS denotes an absolute gaussian where the variation is an absolute quantity, and GAUSS denotes a relative gaussian where the variation is with respect to the mean. For the oxide-thickness PDF example above, equivalent statements would be tox = AGAUSS(5.8n, 0.3n, 3) or tox = GAUSS(5.8n, 0.052, 3), where the 3-σ variation of 0.3n is 5.2% of the mean-value 5.8n.

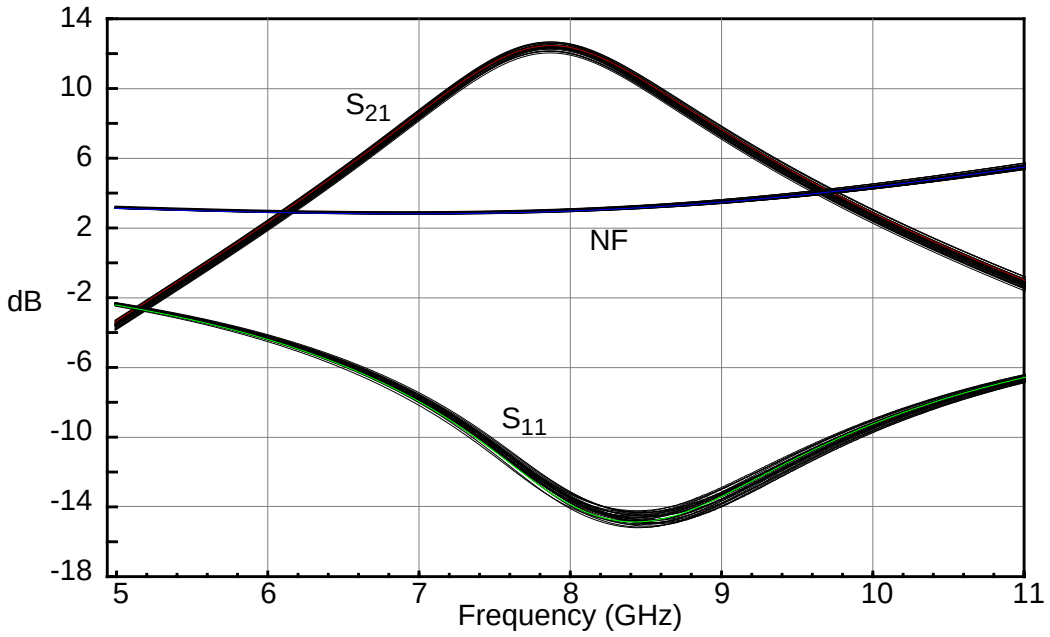


Figure 7-4 Process variation of single-ended LNA's gain (S_{21}), noise figure (NF), and input matching (S_{11}), obtained with Monte Carlo analysis (30 iterations).

7.3.2 LNA and Frequency Divider Variation

Figure 7-4 shows the simulated gain, noise figure (NF), and input-matching (S_{11}) variation for a single-ended low noise amplifier (LNA) from a Monte Carlo simulation with 30 iterations. At 8.5 GHz, the gain (S_{21}) varies by 0.7 dB, the NF varies by 0.2 dB, and the S_{11} varies by 1 dB. The variation in the phase (not shown) of S_{21} is 6^{o}, resulting in a 0.2% skew referenced to the output local clock signal.

Figure 7-5 shows the variation obtained with Monte Carlo simulations of the 8:1 frequency divider for a 500-mV amplitude, 8.5 GHz input signal at V_{dd} = 2 V. At 1 V, the skew is 26 ps at the rising edge and 42 ps at the falling edge. Since the output clock period is ~940 ps (8/8.5 GHz), the skew due to process variation in the frequency divider is 4.5%. To obtain the variability in the self-resonant frequencies of the dividers, a fast-fourier transform was taken on the output signals of the first 2:1 divider when it was

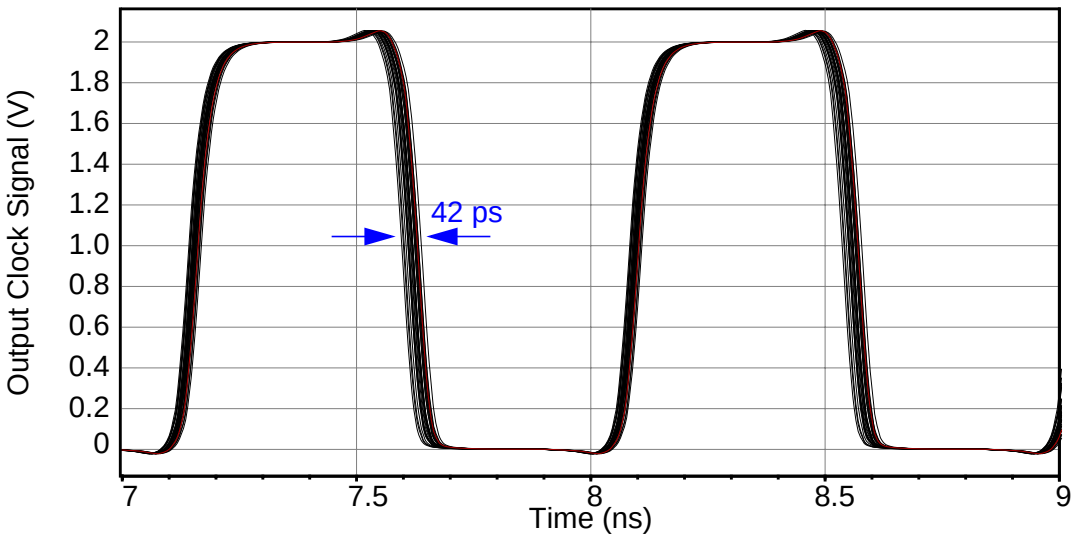


Figure 7-5 Process variation of frequency divider, obtained with Monte Carlo analysis (30 iterations), for an 8.5-GHz, 500-mV amplitude input signal, V_{dd} = 2 V.

self-oscillating. A 640-MHz variation in the output frequency of the 2:1 divider was observed, corresponding to a 1.28-GHz variation in the input-referred self-oscillation frequency, which is significant.

7.3.3 Clock Receiver Variation

The variability of the entire clock receiver was analyzed using both small-signal (AC) analysis and transient analysis. Referring to Figure 1-3(b), the receiver consists of a fully-differential LNA, a pair of source-follower buffers, an 8:1 frequency divider, and output buffers. Figure 7-6(a) shows the simulated gain variation from a Monte Carlo analysis (30 iterations), equal to the voltage gain versus frequency from the input of the receiver to the input of the frequency divider. Due to both the LNA driving a capacitive load and the negative input conductance of the source-followers, the gain is much larger than that of the LNA driving a resistive load. Furthermore, since the resonant frequency of the LNA in the receiver is set by the small input capacitance of the source-follower, the

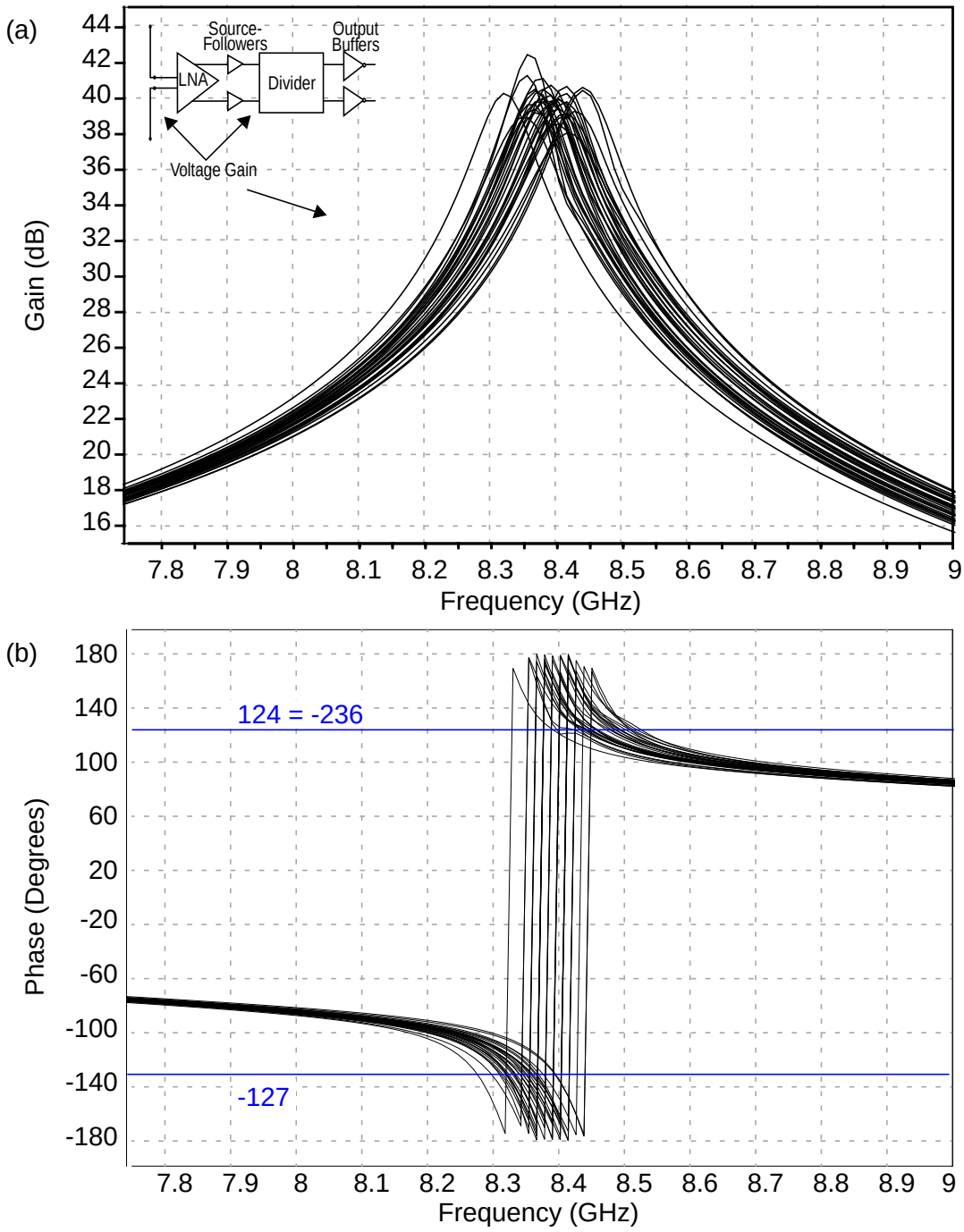


Figure 7-6 Simulated process variation of (a) voltage gain and (b) phase-shift of receiver from antenna input to input of frequency divider.

variation in the resonant frequency can be large. The maximum gain at 8.5 GHz varies from 27 to 36 dB, with the resonant frequency varying by ~120 MHz. As can be seen, the gain variation is primarily due to the resonant frequency shifting, rather than the peak gain

shifting. This 9-dB gain variation is severe, and can result in clock skew due to amplitude mismatch. Referring to section 5.4, Figure 5-5, a 9-dB amplitude variation can result in as much as 23 ps of skew at 8.5 GHz divided by 8, or 2.4% output clock skew.

Additionally, the variation in the resonant frequency will cause different phase-shifts through the amplifier at a given input frequency. Figure 7-6(b) shows the phase-shift to the input of the divider versus frequency. At 8.5 GHz, the variation in phase-shift is 27.6^{o}, yielding 9 ps of output skew or ~1% of the local clock period. The phase variation increases around the resonant frequency, though. At 8.39 GHz, corresponding to the worst-case variation, the phase variation is $\sim 109^{o}$, which is ~30% of the input period and 3.8% of the output period (i.e., 30% divided by 8).

Even more severe than the skew due to amplitude mismatch and resonant frequency variations is the fact that this gain variation can cause the signal at the input of the divider to be too low for the divider to lock. In that case, the divider would self-oscillate, and the system would not be synchronized. The gain variation in Figure 7-6(a) is compounded by the variation in the input sensitivity of the divider. As was just mentioned, the input-referred self-oscillation frequency (f_{iSO}) can vary by ~1.28 GHz. Thus, the conversion gain of the divider, and hence, the gain of the receiver will vary considerably.

Figure 7-7 shows the output clock waveforms from the Monte Carlo simulations (30 iterations) for three different input power levels to the receiver. Reading top to bottom, the input power levels are -16 dBm, -24 dBm, and -31 dBm. At a -16-dBm input power--Figure 7-7(a)--the output clock waveforms are all at the same frequency, which is 8.5 GHz divided by 8 = 1.0625 GHz. The skew at the rising and falling edges are 30 and 36 ps, respectively, which corresponds to a 3.8% skew. At a -24-dBm input power--Figure

7-7(b)--the majority of the output clock waveforms are at 1.0625 GHz, with similar skew to that just mentioned. However, there are a few iterations where the output waveforms are at a different frequency, showing that the divider is self-oscillating. This means that the input signal to the divider is not large enough to lock the divider. Finally, at a -31-dBm input power--Figure 7-7(c)--virtual chaos is evident, with most of the clock waveforms at different frequencies. At this power level, the system has failed.

7.3.4 Conclusions for Process Variation

Table 7-3 summarizes the process variation results. Most significant among these results are the phase-shifts due to process variation, resulting in output clock skew, and the large variation in f_{iSO}. Also, these results show that as the input signal level decreases, the receiver becomes more susceptible to process variation and eventually fails at low input levels. Largely, this problem is due to the input signal level to the divider not being large enough to lock the divider. In other words, this means that the overall receiver gain, consisting of the amplifier and divider conversion gain, has its peak at a different frequency.

These results first motivate the need for some type of automatic gain control (AGC) in the receiver. The AGC circuits could tune the resonant frequency of the amplifier and/or adjust the peak gain level. In so doing, the variation in phase-shift through the amplifier would be controlled as well. Most importantly, the f_{iSO} of the injection-locked frequency divider should be tunable, such that the input signal will always be able to lock the divider. This tunability could be obtained by designing the first 2:1 injection-locked divider as a differential voltage-controlled oscillator (e.g., [Rat99]). Second, these results have been obtained with very primitive biasing techniques. Using more advanced biasing techniques should improve the circuits' immunity to process variation.

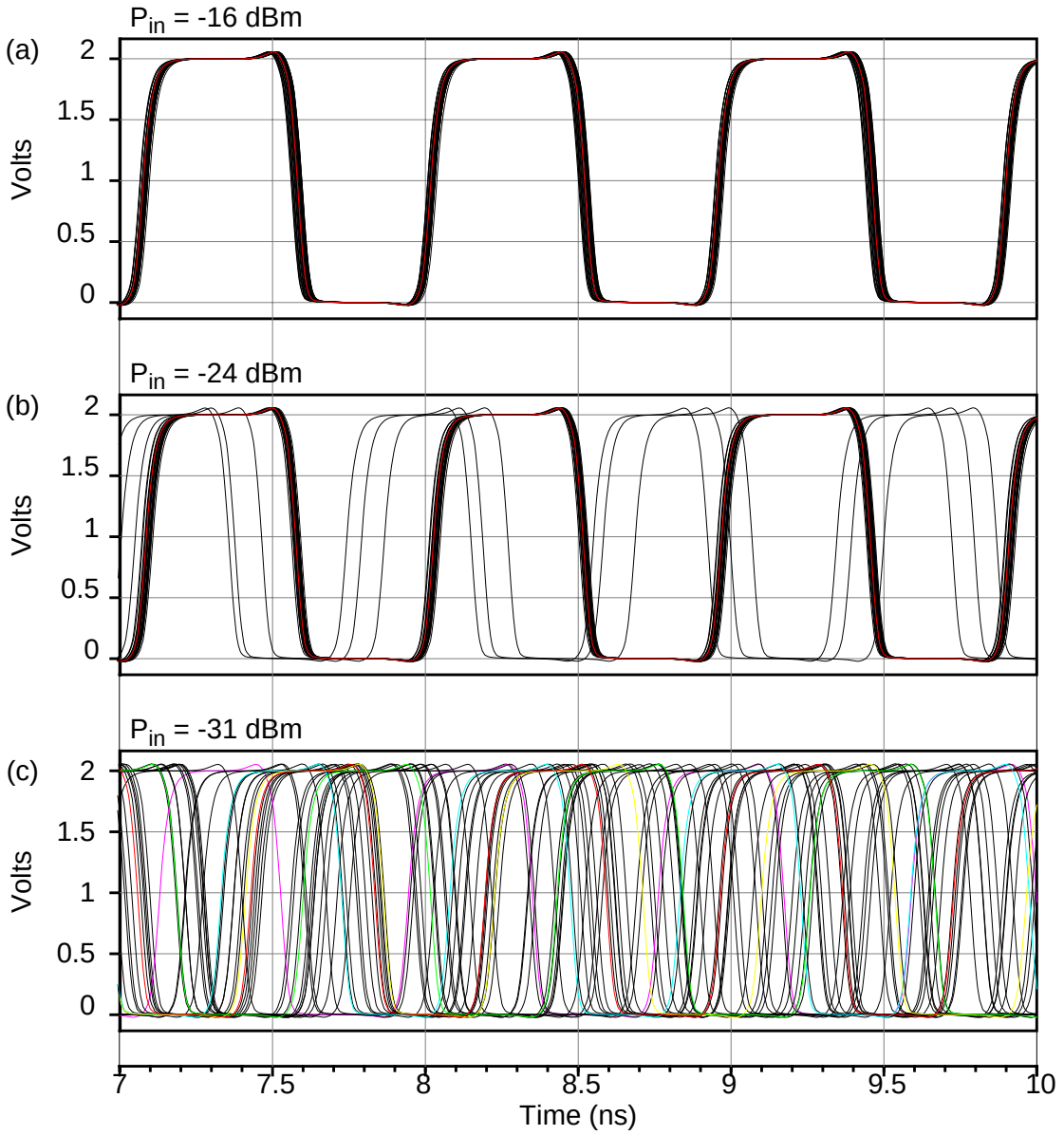


Figure 7-7 Output clock signals from frequency divider with process variation: Input power levels are (a) -16 dBm, (b) -24 dBm, (c) -31 dBm.

7.4 Synchronization

Probably the single-most important criterion for a global clock distribution system is that all of the output clock signals should be synchronized, having low clock skew and low clock jitter. The clock skew should be less than 5-10% of the clock period, while the peak-to-peak clock jitter should be less than 3% of the clock period. This section will look

Table 7-3 Summary of simulated process variation for 0.25-μm receiver circuits.

Parameter	Absolute Variation	Percentage
LNA Gain	0.7 dB	5.7%
Input Matching (S_{11})	1 dB	7.4%
Noise Figure	0.2 dB	6.7%
Divider Output Signals, When Locked	42 ps	4.5% f_{out}=1.0625GHz
Divider f_{iSO}	1.28 GHz	12% (input)
Receiver Gain (to divider input)	9 dB, f_{in} = 8.5 GHz 6.3 dB, f_{in} = 8.39 GHz	28%, f_{in} = 8.5 GHz 16%, f_{in} = 8.39 GHz
Phase-Shift Due To Amplitude Mismatch	69^o, f_{in} = 8.5 GHz 61^o, f_{in} = 8.39 GHz	2.4%, f_{out} = 1.0625 GHz 2.1%, f_{out} = 1.048 GHz
Receiver Phase-Shift (to divider input)	27^o, f_{in} = 8.5 GHz 109^o, f_{in} = 8.39 GHz	1%, f_{out} = 1.0625 GHz 3.8%, f_{out} = 1.048 GHz
Receiver Output Signals	36 ps, P_{in}=-16 dBm	3.8%, f_{out} = 1.0625 GHz
	(Divider Fails at P_{in} = -31 dBm)	

at the main components which contribute to skew and jitter for a wireless clock distribution system, estimate the (current) worst-case skew and jitter, and then these estimates compare with the measured results from Chapter 6.

7.4.1 Clock Skew

For a wireless clock distribution system, the main elements which will contribute to clock skew are as follows: process variation affecting receiver gain and phase-shift; time-of-flight delay mismatches due to the receivers being different distances away from the transmitter; amplitude mismatches at the input of the divider causing AM-to-PM conversion (section 5.4); interference structures located between the transmitting and receiving antennas affecting antenna transmission gain, impedance, and phase-shift; and finally, mismatches between the loads at the clock receiver outputs. The worst-case skew can be estimated as the sum of the mean skew and 3 standard deviations of the random skew, where the variances (σ^2) of all of random skews will add to yield the total skew variance.

The non-random or systematic skew component will be due to time-of-flight (TOF) delay mismatches. Since the receiver locations cannot be precisely known (the evenly-spaced grid of 16 receivers is more conceptual than practical) there can be a situation where the TOF mismatch is half of the input clock period. For example, the speed of light in a silicon-substrate propagation medium[2] is 0.87×10^8 m/s. If the distance between the transmitter and two receivers differs by 2.9 mm plus any integer wavelength (λ_{Si} = 5.8 mm at 15 GHz), then the TOF delay mismatch is 33 ps, which is half of the period of a 15-GHz input signal. Therefore, the worst-case TOF mismatch is 50% with respect to the input signal, resulting in 6.3% of skew with respect to the output signal.

Random skew components will be due to process variation, amplitude mismatches, and load mismatches. The effects of process variation on skew were presented in the previous section. The results show that for the 0.25-μm receiver, the simulated skew due to process variation is 3.8%. This was for the case when the input signal was large enough to lock the receiver, which is a necessary assumption for this analysis. Although the process variation analysis contained skew due to amplitude mismatch generated in the receiver, there will also be amplitude mismatch due to different antenna gains. The longer the path-length, the lower the transmission gain. Also, interference structures will modify the antenna gain further. Referring to section 5.2.2, the specified antenna gains for 0.5- and 1.5-cm distances are -40 and -56 dB, respectively. Metal interference structures have been shown experimentally to degrade the gain by ~7 dB. Thus, there is a maximum of 23 dB of amplitude mismatch at the input of the divider. Applying (5.17), this results in 3% of skew

2. Since multiple paths exist from the transmitting to the receiving antenna, the effective dielectric constant and hence, speed of light, will be between that of silicon and SiO_2.

with respect to the output signal. Finally, mismatches in the load capacitance of the clock receivers will generate clock skew. These capacitances are assumed to be matched to within 1%; thus, the skew due to this mismatch is also 1%.

The total worst-case estimated skew can now be obtained. Since each of the random skew components are independent, the individual variances can be summed. Also, since the numbers listed in the previous paragraph represent 3-σ variations, the total 3-σ variation is equal to $\sqrt{3.8^2 + 3^2 + 1^2}$ = 4.9%. Therefore, the worst-case uncorrected skew for a wireless clock distribution system is estimated to be the mean skew (6.3%) plus the 3-σ random skew (4.9%), resulting in 11.2% skew, with respect to the output signal. This skew estimation assumes that there is no AGC in the receiver. With AGC, the skew due to amplitude mismatch would be eliminated, and the skew due to process variation would be reduced. Assuming that AGC is used, the worst-case skew would be less than 10.2%. Finally, the use of more sophisticated biasing techniques should reduce the process-induced skew further.

As was shown in Chapter 4, programmable dividers can be used to start-up the receiver in a different state and to reduce clock skew. The types of clock skew that can be corrected for include both systematic and random skew, since both are time-invariant. For an 8:1 divider, the skew will be limited to under $\pm\frac{1}{16}$, or 6.25%. Thus, the worst-case skew using a programmable divider is 6.25%, which meets the system specification of less than 5-10% of skew. Note, however, that to correct for the skew using programmable dividers requires a start-up methodology for the clock receivers which would estimate the uncorrected skew using a phase detector, modify the states of the receiver accordingly, and then synchronously release the clock receivers from the initialized state (refer to section

4.6.2). Additionally, this skew correction technique is static; hence, the receivers could accumulate phase errors if, for example, a single clock pulse is missed due to interference. More work is required to analyze this phase-error accumulation.

In Chapter 6, the measured skew between two receivers with programmable dividers was 4.7%. This skew included process variation, TOF delay mismatches, amplitude mismatch, and different interference structures. As expected, the measured skew is less than 6.25%. These results show that the wireless clock distribution system should be able to meet the skew requirements of global clock distribution systems. However, additional work is needed to perfect the start-up technique for the programmable dividers (and correct for the state-dependent initialization failure of the dividers described in 4.6.4). This start-up methodology appears to be the ultimate key for demonstrating feasibility in terms of clock skew for a wireless clock distribution system.

7.4.2 Clock Jitter

The main elements contributing to clock jitter for a wireless clock distribution system are as follows: thermal noise received by the antenna and generated in the receiver and antenna, switching noise or digital interference received by the antenna, power-supply noise, and phase noise from the phase-locked loop (PLL) which synthesizes the global clock signal in the transmitter. Since these sources of jitter are all independent, their variances add. As was shown in Chapter 5, thermal noise and interference degrade the signal-to-noise ratio (SNR) at the input of the frequency divider, resulting in jitter at the output of the divider (given by (5.35)). Noise on the power supplies will translate into noise on the signals themselves, depending on the power-supply-rejection-ratio of the

circuit. Finally, jitter in the source or PLL will correspond to jitter on the output signal, where the jitter as a percentage of the period is divided by 8 through the clock receiver.

Estimations for each of these jitter components will now be presented. First, the jitter due to thermal noise has been simulated with SPICE. As was shown in section 5.7, the simulated SNR due to thermal noise was 21.8 dB, resulting in ~1% of peak jitter. This simulation assumed an input thermal noise of kT. Second, to estimate the amount of interference at the receiver input, digital test circuits or noise generators have been placed very close to antennas [Brav00a, Brav00b], allowing the power spectral density to be obtained. Measurements and simulations in [Brav00a, Brav00b] show that the total power due to digital switching noise is -74 dBm. If the input signal level is at the desired receiver sensitivity of -54 dBm, then the signal-to-interference ratio (SIR) is 20 dB, resulting in 1.2% of peak jitter. Third, since a CMOS PLL has not been built at 15 GHz, the peak jitter of the PLL at 15 GHz is assumed to be 5%. Compared to results found in literature [Yan97, Boe99, Tam00, Kae98, Mai97], this jitter specification should be attainable. With respect to the output divide-by-8 signal, this results in 0.625% of peak jitter. Therefore, the total peak jitter due to thermal noise, interference, and source (PLL) jitter is $\sqrt{1^2 + 1.2^2 + 0.625^2}$ = 1.68%. Since the peak-jitter specification is 3%, this leaves a $\sqrt{3^2 - 1.68^2}$ = 2.5% margin.

The above jitter estimate is optimistic for two main reasons. First, the estimations were made with noiseless or quiet supplies. When the microprocessor is operating, there will be significant noise on the power and ground lines, even with power-supply decoupling. This will generate jitter in both the transmitter and receiver circuits, consuming part of the 2.5% margin. To help offset this jitter, the analog supplies for the wireless clock

distribution system should be independent of the digital supplies. Even still, noise will couple to these supplies from both the digital circuits and the switching of the receivers. Second, the amount of switching noise will most likely be larger than the -74 dBm measured in [Brav00a, Brav00b] (which was for only one noise generating circuit). If the amount of noise is quadrupled--corresponding to noise generators on all four sides of the receiver--then the power would increase to -68 dBm, the SIR would decrease to 14 dB, the peak jitter due to interference would increase to 2.4%, and the total peak jitter would increase to 2.7%. This would only leave 1.3% of peak-jitter margin for the noisy supplies.

In Chapter 6, the measured peak-to-peak jitter, with a quiet supply and without any digital switching noise, was 1.24%. This jitter is due to thermal noise, corresponding to a 19.7 dB SNR. As can be seen, this agrees very well with the estimated peak jitter from thermal noise of 1%, validating both the simulated SNR and the SNR-jitter relationship. Therefore, these results suggest that the peak-to-peak jitter due to thermal noise, interference, and source jitter should be approximately 2.4%, meeting the system specification of 3% peak-to-peak jitter. However, more work is required to quantify how much jitter is introduced by noisy supplies. Also, the jitter from a PLL at 15 GHz should be quantified and checked against the assumed value. If the jitter specification is exceeded by the noisy supplies and the PLL, then the receiver circuitry could be optimized to decrease the jitter due to thermal noise and interference. One potential improvement would be to use a differential LC-oscillator as the first 2:1 injection-locked divider [Rat99]. Due to the higher Q of this circuit as compared to the low Q of a ring oscillator, the output phase noise and, hence, jitter will be decreased. This decrease is due to the filtering provided by the injection-locking, where the output phase can only follow the input phase over a limited locking range, as shown in Appendix E.

7.4.3 Conclusions for Synchronization

This section has estimated the (current) worst-case clock skew and jitter that can be obtained with a wireless clock distribution system. The worst-case uncorrected skew due to process variation, TOF mismatch, amplitude mismatch (from different antenna gains), and mismatches in the output load is estimated to be 11.2%. Using a programmable 8:1 divider, though, will reduce the skew to under 6.25%. This necessitates a start-up methodology to program and release the dividers synchronously. The worst-case peak-to-peak jitter due to thermal noise, switching noise (digital interference), and phase noise on the global clock signal, is estimated to be 2.4%. However, more work is required to evaluate the jitter introduced by power-supply noise and the jitter of a 15-GHz PLL. Measured results of a 15-GHz double-receiver wireless interconnect have shown a clock skew of 4.7% and a peak-to-peak clock jitter of 1.24%. These results help to confirm the estimations made in this section, showing that a wireless clock distribution system should be able to meet the skew and jitter requirements for microprocessors. However, more work is required to validate these estimations and to demonstrate the clock skew and jitter in a working microprocessor (or close proximity thereof).

7.5 Latency of 0.18-μm Wireless Interconnect

The increasing latency of conventional interconnects is a primary motivation for investigating alternative interconnect systems. Therefore, the latency of the 0.18-μm wireless interconnect has been calculated. The latency will include TOF delay and delay through the clock receiver. If the silicon-substrate is assumed as the propagation medium (which would have the worst-case latency due to higher dielectric constant), then the TOF delay for a 1.3-cm propagation distance is 150 ps (this distance is assumed for the 100-nm

technology generation, which has a 2-GHz global clock, and a 622-mm^2 area [SIA99]--for an evenly-spaced grid of 16 receivers, the longest distance from the center to the corner receiver is 1.3 cm.). The latency through the clock receiver was simulated with SPICE, having the following components: LNA and source-follower delay = 30 ps, first 2:1 divider delay = 26 ps, second 2:1 divider delay = 55 ps, and third 2:1 divider delay = 77 ps. Thus, the total latency through the 0.18-μm receiver is 188 ps, and the wireless interconnect has a total latency from the transmitter to the (unbuffered) output of the receiver of approximately 338 ps. This corresponds to 63% of a 1.875-GHz output waveform. The latency through the output buffer was not included since this would depend on the load that the receiver is driving. Also, the delay through this buffer would be the same for any interconnect system, since the local clock loads are equal. A rough estimate of the clock skew could be approximately 10% of the latency, which is 34 ps or 6.3% of the output clock period. This is less than the estimated worst-case skew of 11.2%, and is within the allowable skew range of 5-10%.

The latency through the interconnect is still fairly large. What makes wireless interconnects attractive, though, is that the latency through the receiver will decrease with subsequent technology generations; whereas the latency through conventional interconnect continues to increase (refer to Figure 1-1). For example, scaling from the 100-nm to the 70-nm generation, the gate delay decreases by ~30%, whereas the global interconnect delay increases dramatically [SIA99, Boh95]. The maximum interconnect distance increases according to the square-root of the area increase, or from 1.3 cm to 1.4 cm (7%). The TOF delay therefore increases by 7%, while the delay through the receiver decreases by ~30%. Thus, the wireless interconnect latency will decrease from 338 to 292 ps--a 14%

decrease. This decrease will be lessened when the output buffer latency is included, which will be increasing with each technology generation. However, this example shows that the wireless interconnect latency is decreasing with technology generation, whereas the conventional interconnect latency is increasing.

7.6 Intangibles

While feasibility issues such as power consumption, synchronization, and latency have been quantified, there are other feasibility issues which are harder to quantify, but which contribute to the overall system feasibility. These intangible feasibility issues include the area consumed by the system, and design verification.

Since the wireless clock distribution system employs antennas and active circuitry, there is an area penalty incurred in using wireless interconnects. For the 0.18-μm circuits, the areas of the transmitter and receiver, excluding antenna and pad area, are 0.116 mm^2 and 0.215 mm^2, respectively. Each antenna occupies 0.15 mm^2. For a wireless clock distribution system consisting of one transmitter, 16 receivers, and 17 antennas, the total area consumed is 6.2 mm^2. The ITRS projects the die size of a 0.1-μm generation microprocessor to be 622 mm^2. Thus, ~1% of the microprocessor area will be consumed by the wireless clock distribution system. Approximately half of this area is due to the 2-mm long antennas; thus, more area-efficient antennas would be desirable.

The area consumed by the wireless clock distribution system has to be weighed against the metal area saved. Since the global clock tree will be eliminated, there will be less area consumed by routing global signals. This will then free up more of the top-level metal for the functional blocks across the microprocessor. As a result, their area could

potentially be decreased. Thus, cost-functions for both the active area and the metal area should be developed to evaluate the total area cost of a wireless interconnect system.

Another intangible feasibility item is the ability to accurately verify if the system will function properly, known as design verification. With any global clock distribution system, it is imperative to meet the clock requirements with “first silicon”. For conventional interconnect systems, sophisticated computer aided design (CAD) tools have been developed to model the transmission-line effects, extract the parasitics associated with a line, and model current return-paths. For a wireless clock distribution system, CAD tools would also have to be developed, or at least improved, to model the antenna characteristics, the effects of metal interference structures between the antennas, the digital switching noise, and the RF performance of the circuits (requiring accurate inductor and transistor modelling). While this hurdle is not insurmountable, it is quite large, pointing out the need for additional research.

7.7 Conclusions and Future Work

7.7.1 Feasibility Summary

The feasibility of a wireless clock distribution system has been evaluated, yielding the following results. First, the power consumption of a wireless clock distribution system is similar to that of conventional systems, where the clock receivers and transmitter will consume less than 2% of the system power. Second, the clock skew of the wireless clock distribution system will be less than 6.25%, while the peak-to-peak clock jitter should be less than 3%, and both of these numbers have been verified with measurements. Thus, a wireless system should be able to meet the skew and jitter requirements for clock distribution systems. Third, process variation has been shown to affect both the skew and the basic

operation, where at low input power levels, the system does not operate across all process variations. This necessitates the need to control the gain in the receiver, through adjusting the resonant frequency of the amplifier and adjusting the self-resonant frequency of the injection-locked divider. Fourth, the latency of the system is ~340 ps for a 15-GHz, 0.18-μm wireless interconnect, and future technology scaling will benefit wireless interconnect latency over conventional interconnect latency. Fifth, the wireless clock distribution system will consume approximately 1% of the projected microprocessor area; however, this is offset by the top-level metal area that will be conserved. Sixth, design verification of a wireless clock distribution system is currently difficult, and further work is required. All of these feasibility results are promising, in that none are dissuasive. On the contrary, these results are promising enough to warrant further investigation of larger-scale wireless clock and interconnect systems.

7.7.2 Conclusions for Wireless Clock Distribution Systems

Examining these results, it can be seen that comparable power consumption, skew, and jitter can be obtained with a wireless clock distribution system, as compared to conventional systems, with potential costs of added area and more difficult design verification. The benefits of a wireless clock distribution system, as discussed in Chapter 1, can be summarized as being able to provide high frequency clock signals with little to no dispersion over large distances, where the latency of the interconnect is improving with technology. This should increase the maximum clock frequency of microprocessors. Additionally, these benefits can be obtained using conventional CMOS technology. Thus, while there is a circuit overhead for a wireless clock distribution system, such a system could be used to provide global interconnects for microprocessors operating well above 2500 MHz. In

addition, the upper frequency limit is set by how fast the RF circuits can operate, rather than how fast the interconnects can operate. This is a hidden benefit of wireless interconnects, in that the performance improves as the frequency increases (the improvements are largely due to the antennas and inductors becoming more efficient). Thus, wireless interconnects shift the microprocessor performance from being back-end (i.e., interconnect) limited to once again being front-end (i.e., transistor) limited.

Therefore, this work has demonstrated both the plausibility and feasibility of a wireless clock distribution system. First, the design and implementation of LNA and frequency divider circuits operating between 1 and 24 GHz was presented. The results demonstrate the competitiveness of CMOS for both interconnect and general wireless communication systems. Second, the system requirements of a wireless clock distribution system were derived, translating the clock requirements of skew and jitter into standard radio requirements. Third, the plausibility of a wireless interconnect system was demonstrated by implementing on-chip antenna pairs, clock receivers, and clock transmitters. These are the first demonstrations of wireless interconnects and the first time antennas and circuitry have been incorporated on the same silicon chip. Finally, the feasibility of a wireless interconnect system was evaluated in terms of power dissipation, synchronization, process variation, latency, area, and design verification. All of these results indicate the potential of an on-chip wireless clock distribution system.

7.7.3 Broader Applicability

The results from a wireless clock distribution system can be applied to general wireless interconnect systems as well as RF systems with on-chip antennas. Basically, a wireless clock distribution system consists of communication of just a carrier signal.

Therefore, by modulating this carrier, data communications can be obtained. Such data communications could be used for on-chip interconnection, multi-chip interconnection, and general wireless communications. Obviously, the circuitry will be more complicated; however, this work has shown that CMOS can support RF circuitry operating up to 20 GHz. Also, this work has demonstrated transmitter and receiver circuits with on-chip antennas. Potentially, this could be the largest application for this work, in that a true single-chip radio (including antenna) could be implemented for low-cost applications. Therefore, in summary, this work is applicable to both wireless interconnect systems and general wireless communication systems.

7.7.4 Suggested Future Work

Circuit Design and Implementation. First, the state-dependent initialization failure in the programmable divider has to be corrected using the new latches presented in Figure 4-24. Second, automatic gain (and frequency) control circuits should be implemented in the receiver to tune the gain in the amplifier and the self-oscillation frequency of the injection-locked divider. Potentially, the first 2:1 divider could be changed to an LC injection-locked oscillator. Third, the system's robustness against process variation should be improved by stabilizing or potentially eliminating the source-follower buffer and using more sophisticated biasing techniques for the transmitter and receiver. Finally, a phase-locked transmitter operating above 15 GHz has to be implemented. Particularly, the CMOS PA requires optimization, such that it delivers more power to the antenna.

Antenna Design and Characterization. First, the modeling and predictions of antenna performance should be improved, using three-dimensional electromagnetic simulation tools. This is very important to the overall system operation, since both the antenna

impedance and transmission gain affect the power delivered to the input of the receiver. Second, the area-efficiency of antenna structures should be improved, since, currently, the antennas occupy about as much area as the receiver and transmitter circuits. Third, the substrate antennas should be further examined, simulated, and optimized. Fourth, a test-chip containing more realistic interference structures should be implemented. The test structures should include metal-fill patterns as well as multiple layers of metal. Design rules for the antennas should then be explicitly defined. Finally, a test setup should be developed to analyze how the package affects system performance. The package setup should include solder balls used for flip-chip bonding, ground planes embedded in the package and the board, and the heatsink.

System-Level Implementation and Demonstration. First, the initialization and start-up methodology for the programmable receivers should be developed beyond that presented in Chapter 4. In particular, a method to synchronously release each initialized receiver is required. Using this methodology, a multiple-receiver system should be implemented (which could include phase detectors to measure the static phase error and analog-to-digital converters to translate this phase-error into a specific count for the receiver). Second, the accumulation of phase-errors in the static phase-correction system should be quantified. Third, the jitter due to noisy supplies and realistic switching noise has to be quantified. Finally, an intra-chip wireless clock distribution system consisting of a transmitter and multiple receivers should be used to provide a clock signal to an actual microprocessor core. Using this platform, the clock skew and jitter of the wireless clock distribution can be obtained, and realistic system operation can be demonstrated.

APPENDIX A
THEORY FOR COMMON-GATE LOW NOISE AMPLIFIER

A.1 Input Impedance

Figure A-1 shows the small-signal model of a common-gate low noise amplifier (LNA). By inspection, the input admittance for the common-gate amplifier is

$$Y_{in} = g_m + j\omega C_{gs} + \frac{1}{j\omega L_s}. \tag{A.1}$$

Thus, to achieve an input impedance of ~50 Ω, g_m is set between 1/70 and 1/35 Ω^{-1}, while L_s is chosen to parallel-resonate with C_{gs} at the operating frequency.

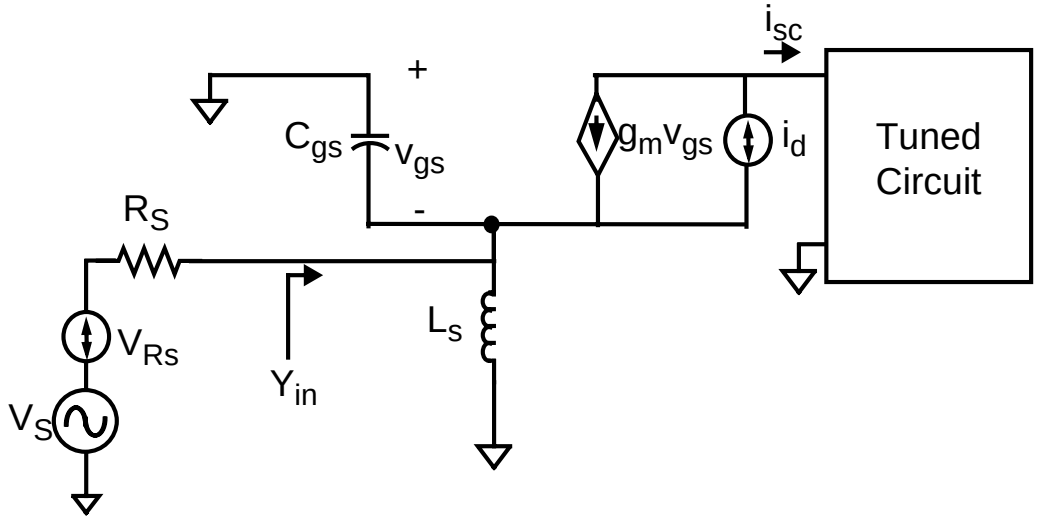


Figure A-1 Small-signal model of common-gate low noise amplifier.

A.2 Gain

To calculate the gain of the common-gate amplifier, the circuit transconductance is first calculated. Assuming that the source inductor parallel resonates with C_{gs1}, the circuit transconductance is as follows:

$$G_m = \frac{i_{d1}}{v_S} = \frac{v_1}{v_S} g_m = g_m \left(\frac{1/g_m}{R_S + 1/g_m} \right) = \frac{g_m}{1 + g_m R_S}. \qquad \text{(A.2)}$$

As can be seen, R_S degenerates the transistor. Therefore, the common-gate LNA is typically more linear than an inductively-degenerated common-source LNA.

For a tuned load output, the S_{21} is equal to

$$|S_{21}| = 2 \cdot |A_v|_{\omega = \omega_o} = \frac{2 g_m |Z_{Leq}(\omega_o)|}{1 + g_m R_S}, \qquad \text{(A.3)}$$

where $Z_{Leq}(\omega_o)$ is equal to the total load impedance at the amplifier output at resonance. Assuming that the output matching network is the same as that used in the source-degenerated LNA (i.e., a Π matching network containing a drain inductor and a capacitive transformer), then

$$|S_{21}| = \frac{g_m Q_{Ld} \omega_o L_d}{1 + g_m R_S} \left| \frac{1}{n(\omega_o)} \right|, \qquad \text{(A.4)}$$

where Q_{Ld} and L_d are the quality factor and inductance of the drain inductor, and $n(\omega_o)$ is a complex capacitive-transformer ratio defined in (2.25).

A.3 Noise Factor

To derive the noise factor of this amplifier, the short-circuit output current is calculated for the entire circuit, including the source resistance. Converting this to a power spectral density (PSD) and taking the ratio of the total PSD to the PSD from the source resistance yields the noise factor.

The thermal noise generated by the source resistance is represented by a voltage source with a PSD given by the following:

$$\overline{v_S^2} = 4kT \cdot R_S. \qquad \text{(A.5)}$$

Neglecting all other sources of noise except the thermal noise in the MOS transistor (lumped only at the drain), the total short-circuit output current can be shown to be

$$i_{sc} = G_m v_{Rs} + \frac{i_d}{1 + g_m R_S}, \tag{A.6}$$

where G_m is defined in (A.2) and i_d is the channel thermal noise lumped at the drain. This drain thermal noise has a PSD of

$$\frac{\overline{i_d^2}}{\Delta f} = 4kT\gamma g_{do}, \tag{A.7}$$

where γ is a bias-dependent parameter (0.67 for long-channel devices), k is Boltzmann's constant (1.38 x 10^{-23} J/K), T is absolute temperature, and g_{do} is the short-circuit drain conductance. Since these two noise sources are uncorrelated, the output PSD is

$$\overline{i_{sc}^2} = G_m^2\left(\overline{v_{Rs}^2} + \frac{\overline{i_d^2}}{g_m^2}\right), \tag{A.8}$$

where (A.2) has been substituted. Therefore, the noise factor is

$$F = 1 + \frac{\overline{i_d^2}}{g_m^2 \overline{v_{Rs}^2}} = 1 + \frac{4kT\gamma g_{do}}{g_m^2(4kTR_S)} = 1 + \frac{\gamma}{\alpha}\cdot\left(\frac{1}{g_m R_S}\right), \tag{A.9}$$

where α is the ratio between the device transconductance (g_m) and the short-circuit drain conductance (g_{d0}).

APPENDIX B
OUTPUT MATCHING USING CAPACITIVE TRANSFORMER

B.1 Two-Element Matching Technique

Multiple methods, both graphical and analytical, exist to quickly match one impedance to another using two reactive elements. An analytical method found in [Bow82] which is both easy to understand, use, and code (i.e., into Matlab), is summarized here for convenience. The simplest matching scenario is matching two resistances using an "L" or two-element network. In this case, the larger resistance, termed R_p, requires a shunt reactive component (decreasing the impedance), while the smaller resistance, termed R_{se}, requires a series reactive component. The sign of these reactances (i.e., inductive or capacitive) are opposite of one another for the net reactance to be zero.

The formulas for this method are as follows:

$$Q = \sqrt{\frac{R_p}{R_{se}} - 1}, \tag{B.1}$$

$$X_s = \pm Q R_{se}, \tag{B.2}$$

$$X_p = \mp \frac{R_p}{Q}, \tag{B.3}$$

where X_s and X_p are the required series and shunt reactances of the L network. An illustration of this procedure is given in Figure B-1. The value of the inductance and capacitance of each component can easily be obtained from the reactance for a given angular frequency. To handle complex sources and loads, the reactance of the source/load is absorbed

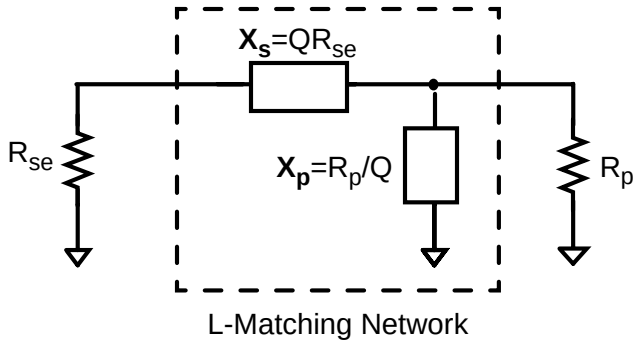


Figure B-1 “L” network matching design.

into the matching network. Hence, the total reactances in the matching network and the source/load should be equal to the values X_s or X_p, as given by (B.2) and (B.3).

B.2 Application to Capacitive Transformer in LNA

Figure B-2 shows the output matching network for the LNA, including the capacitive transformer. Here, the output impedance of the cascode has been modeled by $R_{P2}||C_{P2}$, while the drain inductor is modeled as a parallel network composed of L_d, R_{PLd}, and C_{Ld}. As can be seen, C_1 is the shunt reactance, while C_2 plus the equivalent series reactance from L_d and C_{Ld}+C_{P2} is the total series reactance. Hence, the total impedance at

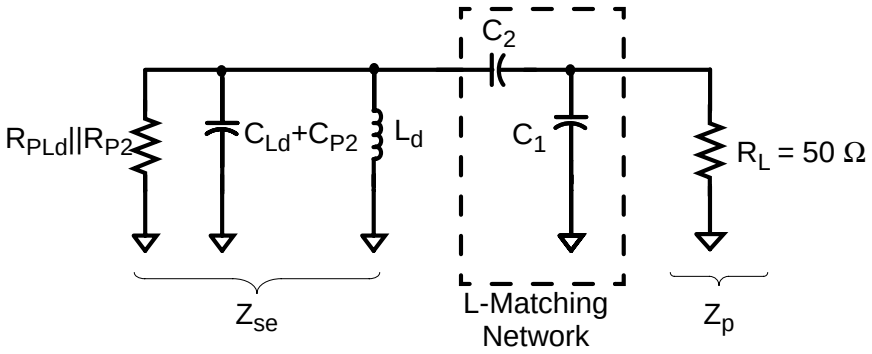


Figure B-2 Small-signal model of common-gate low noise amplifier.

the output of the cascode, Z_{se}, including the drain inductor should first be calculated, as follows:

$$Z_{se} = \left(\frac{1}{R_{PLd} \parallel R_{P2}} + j\omega(C_{Ld} + C_{P2}) - \frac{j}{\omega L_d} \right)^{-1} = R_{se} + jX_{se}, \qquad \text{(B.4)}$$

where R_{se} and X_{se} are the real and imaginary parts of Z_{se}, respectively. Setting $R_p = R_L = 50\ \Omega$, and then using (B.1) yields the quality factor, Q, of the L matching network. Equations (B.2) and (B.3) are then used to find C_2 and C_1, respectively, as follows:

$$C_2 = \frac{1}{\omega(X_{se} - QR_{se})} \qquad \text{(B.5)}$$

$$C_1 = \frac{Q}{50 \cdot \omega}. \qquad \text{(B.6)}$$

If either (or both) of these values is negative, it signifies that an inductor should be used in place of the capacitor. If this is unacceptable for the LNA design, then the value of L_d (and its associated parasitics) should be modified.

APPENDIX C
DERIVATION OF NOISE PARAMETERS

C.1 Equivalent Input Noise Generators

Any "noisy" two-port network can be represented as a "noiseless" two-port network with equivalent voltage (v_n) and current (i_n) noise generators at the input of the network [Gra93], as shown in Figure C-1. The two noise generators allow the noise properties of the network to be correctly represented for any input impedance (admittance). To calculate these noise generators, the output short-circuit (i_{sc}) current can be equated for both networks with the input first short-circuited and then open-circuited, yielding v_n and i_n, respectively.

Traditionally, the noise factor of the network is characterized in terms of four noise parameters, as follows:

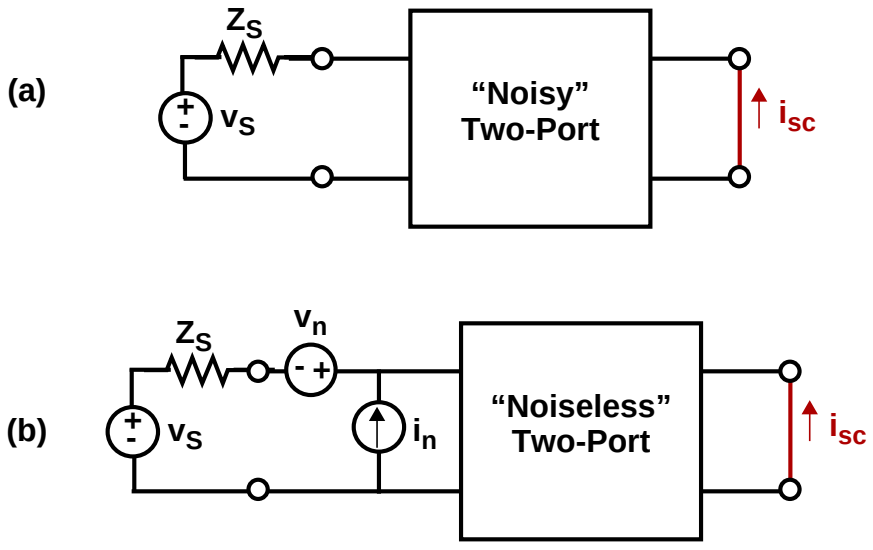


Figure C-1 Representation of a "noisy" two-port network as a "noiseless" two-port with equivalent input noise generators.

$$F = F_{min} + \frac{R_n}{G_S}[|Y_S - Y_{opt}|^2], \tag{C.1}$$

where F_{min} is the minimum obtainable noise factor, R_n is the noise conductance, $Y_{opt} = G_{opt} + jB_{opt}$ is the optimum source admittance resulting in $F = F_{min}$, and $Y_S = G_s + jB_S$ is the actual source admittance. These noise parameters are easily derived from the input noise generators, and they assume that the input is in an admittance form. However, for cases when the input is in an impedance form (e.g., for a source-degenerated LNA), it is advantageous to represent the noise parameters in an impedance form as well. Such a representation yields design insight, since the optimal noise factor will occur when the voltage-source impedance is equal to the optimum noise impedance. Unfortunately, most electronics textbooks only represent the noise parameters in an admittance form; therefore, the impedance form of these parameters is derived here.

C.2 Noise Parameters in Impedance Form

Assume that the two-port network is represented using equivalent input noise generators, as shown in Figure C-1(b). A source with an impedance $Z_S=R_S+jX_S$ is connected to the input and generates an input thermal noise of

$$\overline{v_S^2} = 4kTR_S\Delta f, \tag{C.2}$$

where k is Boltzmann's constant (1.38×10^{-23} J/K) and T is the absolute temperature in Kelvin. The noise factor of the network is then equal to the total input-referred noise divided by the noise generated at the input by the source, as follows:

$$F = \frac{\overline{v_S^2} + \overline{|v_n + i_n Z_S|^2}}{\overline{v_S^2}}. \tag{C.3}$$

To account for correlation between v_n and i_n, v_n can be divided into components which are correlated (v_c) and uncorrelated (v_u) with i_n, as follows:

$$v_n = v_u + v_c = v_u + Z_c i_n . \tag{C.4}$$

The correlation impedance, Z_c, is

$$Z_c = \frac{\overline{i_n^* v_n}}{\overline{i_n^2}} . \tag{C.5}$$

The power spectral densities of each of these noise sources (i_n, v_u) can be represented by either a resistance (for v_u) or a conductance (for i_n), as follows:

$$G_n = \frac{\overline{i_n^2}}{4kT\Delta f} , \tag{C.6}$$

$$R_u = \frac{\overline{v_u^2}}{4kT\Delta f} , \tag{C.7}$$

where R_u can be obtained using the equivalent input noise generators, as follows:

$$R_u = \frac{\overline{v_n^2}}{4kT\Delta f} - |Z_c|^2 G_n = R_n - |Z_c|^2 G_n . \tag{C.8}$$

Substituting (C.2), (C.4), (C.6), and (C.7) into (C.3) yields

$$F = 1 + \frac{\overline{|v_u + i_n(Z_S + Z_c)|^2}}{\overline{v_S^2}} = 1 + \frac{R_u}{R_S} + \frac{G_n}{R_S}|Z_S + Z_c|^2 . \tag{C.9}$$

Taking the partial derivatives of (C.9) with respect to the source resistance and reactance, and setting the results equal to zero gives the optimum source impedance resulting in minimum noise factor, as follows:

$$R_{opt} = \sqrt{\frac{R_u}{G_n} + R_c^2} \tag{C.10}$$

$$X_{opt} = -X_c . \tag{C.11}$$

The minimum noise figure (F_{min}) can now be obtained by plugging in (C.10) and (C.11) into (C.9), as follows:

$$F_{min} = 1 + 2G_n(R_{opt} + R_c) . \tag{C.12}$$

Thus, the total noise factor can be represented as

$$F = F_{min} + \frac{G_n}{R_S}[|Z_S - Z_{opt}|^2] , \tag{C.13}$$

where the noise parameters in impedance form are F_{min}, G_n, and Z_{opt}.

C.3 Alternative Noise Parameters

The noise performance of any two-port network can be represented by any four noise parameters (e.g., [F_{min}, G_n, R_{opt}, X_{opt}], [F_{min}, R_n, G_{opt}, B_{opt}], etc.). Surveying the results in the previous section, an alternative set of parameters which come directly from the equivalent input noise generators can be defined, from which any other noise parameter set can be easily obtained. These alternative parameters are R_n, G_n, and P_n, where G_n is given by (C.6), while

$$R_n = \frac{\overline{v_n^2}}{4kT} \tag{C.14}$$

$$P_n = \frac{\overline{i_n^* v_n}}{4kT} . \tag{C.15}$$

Here, P_n is a dimensionless correlated “power ratio.” These parameters naturally are needed when trying to obtain any of the traditional noise parameters; thus, they are convenient for numerical techniques. Examining these new parameters, it can easily be shown that

$$Z_c = \frac{\overline{i_n^* v_n}}{\overline{i_n^2}} = \frac{P_n}{G_n}, \tag{C.16}$$

or alternatively,

$$Y_c = \frac{\overline{v_n^* i_n}}{\overline{v_n^2}} = \frac{P_n^*}{R_n}. \tag{C.17}$$

Finally, to obtain F_{min}, the following relationships are used:

$$\begin{aligned} F_{min} &= 1 + 2G_n(R_{opt} + R_c) = 1 + 2G_n R_c + 2\sqrt{G_n R_u + G_n^2 R_c^2} \\ &= 1 + 2Re(P_n) + 2\sqrt{G_n(R_n - |Z_c|^2 G_n) + Re^2(P_n)} \\ &= 1 + 2Re(P_n) + 2\sqrt{G_n R_n - |P_n|^2 + Re^2(P_n)} \\ &= 1 + 2Re(P_n) + 2\sqrt{G_n R_n - Im^2(P_n)} \end{aligned} \quad . \tag{C.18}$$

Thus, R_n, G_n, and P_n can be used to obtain any of the other noise parameters. Through the author's experience, these alternative parameters are more convenient for derivations and numerical techniques, particularly for derivations of F_{min}.

APPENDIX D
NOISE PARAMETERS OF MOSFET

D.1 Transistor Model and Equivalent Input Noise Generators

In this appendix the noise parameters of a single intrinsic MOSFET are derived, including the effects of thermal noise in the channel, lumped both at the gate (gate-induced noise--GIN) and the drain, substrate resistance, and all of the parasitic capacitances. Figure D-1 shows a high-frequency, quasi-static model of the MOSFET [Tsi99] including noise sources. The noise sources have the following power spectral densities:

$$\frac{\overline{i_d^2}}{\Delta f} = 4kT\gamma g_{do}, \tag{D.1}$$

$$\frac{\overline{i_g^2}}{\Delta f} = 4kT\delta\left(\frac{\omega^2 C_{gs}{}^2}{5g_{do}}\right), \tag{D.2}$$

$$\frac{\overline{i_{Rb}^2}}{\Delta f} = \frac{4kT}{R_b}, \tag{D.3}$$

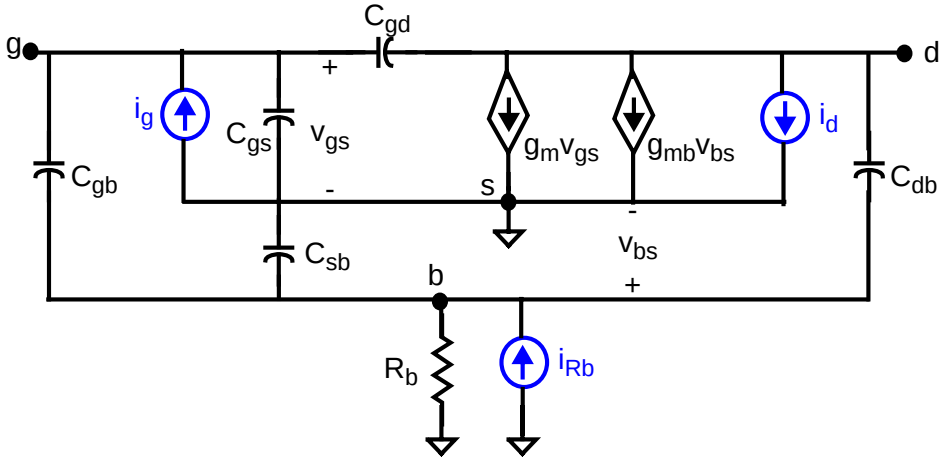


Figure D-1 High-frequency, quasi-static model of intrinsic MOSFET [Tsi99].

where γ and δ are bias-dependent parameters, k is Boltzmann's constant, T is absolute temperature, and g_{do} is the short-circuit drain conductance. The polarity of the noise sources i_d, and i_{Rb} is arbitrary; however, the polarity of i_g should be taken opposite to i_d to yield a correlation coefficient with the correct polarity, equal to

$$c = \frac{\overline{i_g i_d}^*}{\sqrt{|i_g|^2 |i_d|^2}}. \tag{D.4}$$

For long-channel devices, c is purely imaginary, taking a value c=j0.395.

As discussed in Appendix C, any *noisy* two-port network can be represented as a *noiseless* two-port network which has equivalent voltage (v_n) and current (i_n) noise generators at the input of the network. Once these noise generators are obtained, the noise parameters can be derived as discussed in Appendix C. To obtain v_n, the output short-circuit current (i_{sc}) is equated for both a noisy (Figure D-1 as shown) and noiseless network (Figure D-1 containing v_n and i_n at the input and excluding i_g, i_d, and i_{Rb}) when the input is short-circuited. To obtain i_n, the same procedure is followed except the input is now open-circuited. The results are as follows:

$$v_n = \frac{i_d}{y_{21}} + \frac{i_{Rb}}{y_{21}}\left(\frac{g_{mb} - j\omega C_{db}}{Y_b}\right) \tag{D.5}$$

$$i_n = \frac{i_d}{y_{21}}\left(\frac{(\omega C_{gb})^2}{Y_b} + j\omega C_{GT}\right) + i_g + i_{Rb}\left(\frac{j\omega C_{gb}}{Y_b}\right). \tag{D.6}$$

A transadmittance, y_{21}, referring output current to input voltage, is found to be

$$y_{21} = \left.\frac{i_{out}}{v_g}\right|_{v_{out}=0} = g_m(1 + \eta A) - j\omega(C_{gd} + AC_{db}). \tag{D.7}$$

In these equations, A is the voltage division ratio between v_{gs} and v_{bs}, Y_b is the admittance at the body node, η is the ratio between g_{mb} and g_m, α is the ratio between g_m and g_{do}, and C_{GT} is the total gate capacitance. Expressions for these variables are as follows:

$$A = \frac{v_{bs}}{v_{gs}} = \frac{j\omega C_{gb}}{Y_b}, \tag{D.8}$$

$$Y_b = \frac{1}{R_b} + j\omega(C_{gb} + C_{sb} + C_{db}) \equiv \frac{1}{R_b}[1 + j(\omega/\omega_B)], \tag{D.9}$$

$$\eta = \frac{g_{mb}}{g_m}, \tag{D.10}$$

$$\alpha = \frac{g_m}{g_{do}}, \tag{D.11}$$

$$\omega_B = [R_b(C_{gb} + C_{sb} + C_{db})]^{-1}, \tag{D.12}$$

$$C_{GT} = C_{gs} + C_{gd} + C_{gb}. \tag{D.13}$$

D.2 Noise Parameters for Complete Model

Using (D.5) and (D.6), noise parameters for the MOSFET including all second-order effects can be derived, as outlined in Appendix C. The alternative noise parameters (R_n, G_n, and P_n), defined in (C.6), (C.14), and (C.15), are given in Table D-1, where

$$\Phi_B = \left(\frac{1 + [\omega C_{db}/(\eta g_m)]^2}{1 + (\omega/\omega_B)^2}\right). \tag{D.14}$$

As can be seen by examining (D.15), (D.16), and (D.17), the gate-to-body capacitance greatly complicates all of the equations.

These alternative noise parameters can then be used to find more conventional noise parameters, using (C.16) for Z_c, (C.8) for R_u, (C.10) for R_{opt}, (C.11) for X_{opt}, and

Table D-1 Alternative noise parameters for complete MOSFET model

$R_n = \frac{\gamma g_{do}}{\lvert y_{21}\rvert^2} + \eta^2 R_b \Phi_B \left(\frac{g_m}{\lvert y_{21}\rvert}\right)^2$	(D.15)
$G_n = \frac{\gamma g_{do}}{\lvert y_{21}\rvert^2}\left\{\omega^2 C_{GT}^2 + \frac{\omega^4 C_{gb}^4}{\lvert Y_b\rvert^2} + 2\omega^2 C_{gb}^2 \cdot Re\left[\frac{-j\omega C_{GT}}{Y_b}\right]\right\} + \frac{\omega^2 C_{gb}^2}{R_b \lvert Y_b\rvert^2}$ $+ \frac{\gamma g_{do}}{\lvert y_{21}\rvert^2}\left\{\frac{\lvert y_{21}\rvert^2}{g_m^2}\omega^2 C_{gs}^2 \Delta^2 + 2\Delta\lvert c\rvert\omega C_{gs} \cdot Re\left[\frac{y_{21}^*}{g_m}\left(\omega C_{GT} - \frac{j\omega^2 C_{gb}^2}{Y_b}\right)\right]\right\}$	(D.16)
$P_n = \frac{\gamma g_{do}}{\lvert y_{21}\rvert^2}\left\{-j\left[\omega C_{GT} + \left(\frac{y_{21}^*}{g_m}\right)\Delta\lvert c\rvert\omega C_{gs}\right] + \frac{\omega^2 C_{gb}^2}{Y_b^*}\right\} - \left(\frac{j\omega C_{gb}(g_{mb} - j\omega C_{db})}{R_b \lvert Y_b\rvert^2 y_{21}}\right)$	(D.17)

(C.18) for F_{min}. Now that explicit equations are in hand for the noise parameters for the complete model of a MOSFET, a numerical simulator (e.g., Matlab) can be utilized to probe the effect of each model parameter on the noise parameters. Graphical results for this exercise are shown in Figure 2-7. Further intuition can be gained by looking at case studies considering the noise parameters for various second-order effects, while neglecting all other second-order effects, as discussed in the next section.

D.3 Case Studies: Noise Parameters for Second-Order Effects

D.3.1 Case 1 - Effect of C_{gd}

The simplest case for evaluating the noise parameters is to consider the first-order effect, which is thermal noise at the drain (i_d), as well as the effect of C_{gd}. Substrate resistance and all other capacitances except C_{gs} are neglected. Under these assumptions, $y_{21} = g_m - j\omega C_{gd}$, $C_{GT} = C_{gs} + C_{gd}$, and the input noise generators become

$$v_{n1} = \frac{i_d}{y_{21}} = \frac{i_d}{g_m - j\omega C_{gd}} \tag{D.18}$$

$$i_{n1} = \frac{i_d}{y_{21}}(j\omega C_{GT}) = \frac{i_d}{1 - \frac{j\omega C_{gd}}{g_m}}\left(\frac{j\omega}{\omega_T}\right), \quad \text{(D.19)}$$

where the cutoff frequency of the MOSFET is equal to

$$\omega_T = \frac{g_m}{C_{gs} + C_{gd}}. \quad \text{(D.20)}$$

The alternative and impedance-based noise parameters are easily obtained and are shown in the following table, D-2. To obtain the noise parameters without C_{gd}, simply set C_{gd}=0.

Table D-2 Noise parameters considering C_{gd}

Alternative Noise Parameters	Impedance-Based Noise Parameters
$R_{n1} = \frac{\gamma}{\alpha^2 g_{do}\left[1 + \left(\frac{\omega C_{gd}}{g_m}\right)^2\right]}$ (D.21)	$F_{min1} = 1$ (D.22)
$G_{n1} = R_{n1}(\omega C_{GT})^2 = \gamma g_{do}\left(\frac{\omega}{\omega_T}\right)^2 \frac{1}{\left[1 + \left(\frac{\omega C_{gd}}{g_m}\right)^2\right]}$ (D.23)	
$P_{n1} = R_{n1}(-j\omega C_{GT})$ (D.24)	$Z_{opt1} = j\frac{1}{\omega C_{GT}}$ (D.25)

Looking at these noise parameters, it can first be seen that the optimal source impedance is an inductor which series resonates with C_{gs}. Second, the optimal source resistance is a short, meaning that when driving the network with a resistive load, a noise mismatch occurs. Furthermore, F_{min} = 1, meaning that with perfect noise matching (i.e., R_S=0), the MOSFET does not add noise. This is due to there being only one noise source, which is fully correlated to itself; hence, R_u = 0, while R_c = 0 as well. However, F_{min} = 1 is physically unreasonable, meaning that second-order effects will determine F_{min}.

D.3.2 Case 2 - Effect of GIN

The effect of GIN is now analyzed, while neglecting substrate resistance and all other capacitances except C_{gs}. Under these assumptions, $y_{21} = g_m$, $C_{GT} = C_{gs}$, and the input noise generators become

$$v_{n2} = \frac{i_d}{g_m} \tag{D.26}$$

$$i_{n2} = i_d\left(\frac{j\omega}{\omega_T}\right) + i_g . \tag{D.27}$$

The noise parameters can then be derived, and are given in the following table, D-3.

Table D-3 Noise parameters considering GIN

Alternative Noise Parameters	Impedance-Based Noise Parameters
$R_{n2} = \frac{\gamma}{\alpha^2 g_{do}}$ (D.28)	$F_{min2} = 1 + 2\left(\frac{\omega}{\omega_T}\right)\frac{\gamma\Delta}{\alpha}\sqrt{1-\lvert c\rvert^2}$ (D.29)
$G_{n2} = R_{n2}(\omega C_{gs})^2 b_2 = \gamma g_{do}\left(\frac{\omega}{\omega_T}\right)^2 b_2$ (D.30)	
$P_{n2} = R_{n2}(-j\omega C_{gs})b_1$ (D.31)	$Z_{opt2} = \frac{\Delta\sqrt{1-\lvert c\rvert^2}}{\omega C_{gs} b_2} + j\left(\frac{b_1}{b_2}\right)\left(\frac{1}{\omega C_{gs}}\right)$ (D.32)

The following variables have been introduced:

$$b_1 = 1 + \Delta|c| , \tag{D.33}$$

$$b_2 = 1 + 2\Delta|c| + \Delta^2 , \tag{D.34}$$

$$\Delta = \sqrt{\frac{\delta\alpha^2}{5\gamma}} . \tag{D.35}$$

Examining this set of noise parameters, it can first be seen that the inclusion of GIN causes the optimal source reactance to slightly decrease. This means that series

resonance should occur at a higher frequency, as indicated in [Sha97]. Second, an optimal source resistance is now present, causing F_{min} to be greater than one. This is due to the drain and gate noises not being fully correlated. Third, F_{min} is proportional to ω/ω_T, meaning that as technologies scale to shorter channel lengths, lower noise figures will occur for a given operating frequency. Fourth, the optimal source impedance is directly proportional to Q_{gs}, where Q_{gs} is defined in (2.11). This means that as the device becomes smaller (or frequency decreases), Q_{gs} and Z_{opt} both increase.

D.3.3 Case 3 - Effect of R_b, Excluding C_{gb}

Substrate resistance generates thermal noise which is coupled into the device through bulk transconductance and bulk capacitances (C_{gb}, C_{db}, C_{sb}). The inclusion of C_{gb} complicates the equations considerably; therefore, the equations for the full model should be used to examine the effect of C_{gb} on noise. Neglecting C_{gb} and C_{gd}, then $y_{21} = g_m$, A = 0, and $C_{GT} = C_{gs}$. The bulk admittance, Y_b, is defined in (D.9), where $C_{gb} = 0$. This results in the following input noise generators:

$$v_{n3} = \frac{i_d}{g_m} + \frac{i_{Rb}}{g_m}\left(\frac{g_{mb} - j\omega C_{db}}{1 + j(\omega/\omega_B)}\right)R_b \qquad \text{(D.36)}$$

$$i_{n3} = i_d\left(\frac{j\omega}{\omega_T}\right). \qquad \text{(D.37)}$$

The noise parameters can then be derived, and are given in the following table, D-4, where Φ_B accounts for the effect of bulk capacitance on noise.

Examining these noise parameters, it can first be seen that substrate resistance changes R_{opt}, while leaving X_{opt} unmodified. Second, F_{min} has a non-monotonic relationship with R_b, peaking at a certain value of R_b. For R_b=0, $\Phi_B R_b$=0, and hence F_{min} = 1. On

Table D-4 Noise parameters considering substrate resistance and excluding C_{gb}

Alternative Noise Parameters	Impedance-Based Noise Parameters
$R_{n3} = \frac{\gamma}{\alpha^2 g_{do}} + \eta^2 R_b \Phi_B$ (D.38)	$F_{min3} = 1 + 2\left(\frac{\omega}{\omega_T}\right)\eta\sqrt{\frac{\gamma}{\alpha}\Phi_B g_m R_b}$ (D.39)
$G_{n3} = \gamma g_{do}\left(\frac{\omega}{\omega_T}\right)^2$ (D.40)	
$P_{n3} = \frac{\gamma}{\alpha^2 g_{do}}(-j\omega C_{gs})$ (D.41)	$Z_{opt3} = \frac{\eta}{\omega C_{gs}}\sqrt{\frac{\alpha}{\gamma}\Phi_B g_m R_b} + j\left(\frac{1}{\omega C_{gs}}\right)$ (D.42)

the other hand, for very large R_b, F_{min} approaches 1 as well (the limit of $\Phi_B R_b$ as R_b approaches infinity is zero, since Φ_B approaches zero faster than R_b approaches infinity). F_{min} is larger than 1 for R_b values in between 0 and infinity. This shows that short- or open-circuiting the substrate is valuable for minimizing noise figure. This is the case for most other RF performance metrics as a function of substrate resistance. For $C_{db} \sim C_{gs}$, $\eta = 0.25$, and $\omega/\omega_T \sim 0.25$, F_{min} peaks at around 500 Ω. For this case, the substrate resistance range between 40 and 10 kΩ should be avoided if possible to minimize F_{min}.

Care must be taken in trying to obtain the noise parameters as a function of only R_b and drain noise (i.e., neglecting all bulk capacitances). On first glance, it seems that this can be achieved by setting $\Phi_B = 1$. However, this will only match for small values of R_b. The characteristic of decreasing F_{min} for very large values of R_b will not be obtained, since Φ_B should approach zero as R_b approaches infinity. This means that for large values of R_b, the bulk capacitances (C_{db} and C_{sb}) cannot be neglected.

APPENDIX E
INJECTION LOCKING OF OSCILLATORS

E.1 Overview

Any oscillator can be locked or synchronized to an external signal whose frequency (or harmonic) is close to the natural frequency of the oscillator. This type of circuit is known as an injection-locked oscillator (ILO), where the oscillator is locked to either the fundamental, subharmonic, or superharmonic of the natural oscillating frequency. The first presentation of ILOs was by Adler in 1946 [Adl46], where he developed a differential equation relating the phase difference between the locking (input) and oscillator (output) signals for small-level input signals near the natural frequency of the oscillator. From this, the locking frequency range and voltage levels were related, and then the transient pull-in process was investigated. This theory was extended by [Pac65] to accommodate large input-locking levels. The noise properties of ILOs have also been investigated, where the ILO behaves as a first-order phase-locked loop with regards to noise on the input locking signal [Kur68, Llo98]. Multiple other investigations and applications of ILO's exist [Sch71, Uzu85, Zha92, Rat99], and ILOs remain a topic of active research.

The function of this appendix is to review the basic operation of an ILO and to emphasize the results that are important for clock receivers which utilize a superharmonic ILO in the frequency divider. Therefore, the basic differential equation for the phase offset between the input and output signals will be reviewed, followed by a presentation of the locking range, its dependence on signal level, and the steady-state phase error between the

input and output signals. This theory is a summary of the relevant results presented in [Adl46] and [Pac65]. Finally, the phase noise of the ILO will be presented.

E.2 Theory for Injection Locking

E.2.1 Basic Model

Figure E-1(a) shows the basic model for an ILO. Here, the oscillator is modeled simply as a feedback network with a forward path of H(s). This model can therefore be applied to either LC oscillators or ring oscillators. In the absence of an input signal, the circuit will oscillate at its natural frequency, ω_o. At this resonant frequency and only at this frequency, the output of the circuit, V_O, and the error signal, E, are in phase. When a locking signal with amplitude V_L is injected into the loop at a frequency $\omega_L = \omega_o + \Delta\omega$, a different error signal is produced which is phase-shifted (and magnitude-shifted) with respect to V_O. The loop will then oscillate at a frequency where the phase-shift through H(s) is the opposite of the phase-shift induced between V_O and E.

Phasor representations can be used to illustrate the circuit operation, where E is the vector sum of the phasors V_L and V_O, as shown in Figure E-1(b). Here, V_L is assumed to

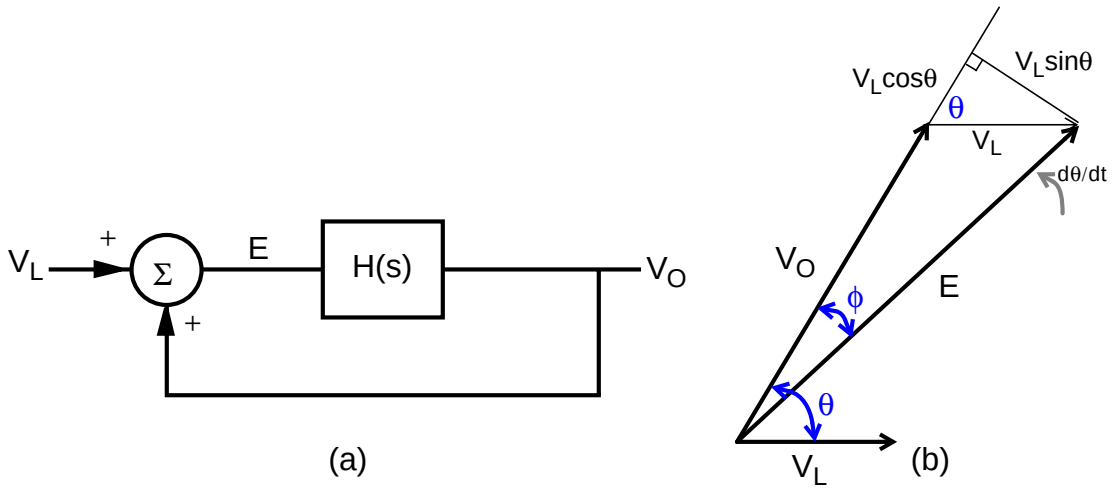


Figure E-1 (a) Basic feedback model of an injection-locked oscillator.
(b) Phasor representation of the system.

be at rest with respect to the observer; thus, the plane itself is rotating at an angular frequency of ω_L. Alternately, the actual sinusoidal voltage signals will be the projection of these phasors onto a line which is rotating at ω_L. Both V_O and E will rotate in this reference plane at a velocity of $\frac{d\theta}{dt}$, corresponding to an angular frequency of $\omega_L+\frac{d\theta}{dt}$.

E.2.2 Differential Locking Equation

From Figure E-1(b), ϕ can be related to θ, V_L, and V_O by the following:

$$\tan\phi = \frac{V_L \sin\theta}{V_O + V_L \cos\theta}. \tag{E.1}$$

The open-loop oscillator circuit--that which is represented by H(s)--is assumed to be generating a phase shift which decreases linearly versus frequency around the band of interest. The slope of this phase versus frequency response is

$$A = \left|\frac{d\phi}{d\omega}\right|. \tag{E.2}$$

For a tuned circuit with quality factor, Q, $A = (2Q)/\omega_o$. Therefore, at an input frequency of $\omega=\omega_L+\frac{d\theta}{dt}$, H(s) generates a phase shift (with respect to the phase at ω_o) of

$$\phi = -A(\omega - \omega_o) = -A\left(\omega_L + \frac{d\theta}{dt} - \omega_o\right) = -A\left(\frac{d\theta}{dt} - \Delta\omega_o\right), \tag{E.3}$$

where $\Delta\omega_o$ is the difference between the natural and locking frequencies (ω_o-ω_L). Plugging this into (E.1) and making a small-angle approximation of $\tan\phi = \phi$, results in the locking equation for an ILO, as follows [Adl46, Pac65]:

$$\frac{d\theta}{dt} = \Delta\omega_o - \left(\frac{1}{A}\cdot\frac{V_L}{V_O}\right)\cdot\frac{\sin\theta}{1+(V_L/V_O)\cos\theta}. \tag{E.4}$$

E.2.3 Locking Range and Locking Signal Level

The ILO is locked when θ is constant, which is when $\frac{d\theta}{dt} = 0$. Therefore, the locking range, $\Delta\omega_o$, can be obtained from (E.4), as follows:

$$\Delta\omega_o = \left(\frac{1}{A} \cdot \frac{V_L}{V_O}\right)\frac{\sin\theta}{1 + (V_L/V_O)\cos\theta}. \qquad \text{(E.5)}$$

For small input locking signals ($V_L << V_O$), this locking range reduces to

$$\Delta\omega_o = \left(\frac{1}{A} \cdot \frac{V_L}{V_O}\right)\sin\theta. \qquad \text{(E.6)}$$

As can be seen, the locking range increases as V_L increases. Also, as the slope of the phase shift versus frequency decreases, the locking range increases. This corresponds to a lower effective Q of the circuit. The required input locking signal level can be obtained from (E.4), by knowing that |sin θ| is always less than 1, resulting in the following:

$$\frac{V_L}{V_O} > \Delta\omega_o A. \qquad \text{(E.7)}$$

E.2.4 Steady-State Phase Error

The steady-state phase error between the input locking signal and the ILO output signal is given as follows [Pac65]:

$$\theta_{ss} = \sin^{-1}\left(\frac{\Delta\omega_o A}{\frac{V_L}{V_O}\sqrt{1 + (\Delta\omega_o A)^2}}\right) + \sin^{-1}\left(\frac{\Delta\omega_o A}{\sqrt{1 + (\Delta\omega_o A)^2}}\right). \qquad \text{(E.8)}$$

At the natural frequency of the ILO, θ_{ss} is zero. This steady-state phase error will result in a skew for the ILO when it is used as a frequency divider in the clock receiver. This skew will depend on the signal level of the injected signal, V_L. For a superharmonic ILO used as

a frequency divider, this phase difference will be with respect to the input frequency; thus, the output steady-state phase error is that given in (E.8) divided by N.

E.3 Phase Noise of Injection-Locked Oscillators

The phase transfer-function of an ILO with a noisy signal, with amplitude V_n, added at the input can be shown to be [Llo98, Rat99, Kur68]

$$\frac{\Phi_{out}}{\Phi_{in}} = \frac{\frac{V_L}{A \cdot V_O}\cos\theta_{ss}}{s + \frac{V_L}{A \cdot V_O}\cos\theta_{ss}} \cdot \frac{V_n}{V_L}. \tag{E.9}$$

The last term, V_n/V_L, represents the input phase noise. The division by the input injected power level is due to the conversion from input additive noise to phase noise [Ega90]. Taking the magnitude squared of (E.9), the output phase noise of the ILO is

$$S_{out}(\omega) = \frac{S_{in}(\omega)}{1 + \left(\frac{\omega}{B}\right)^2}, \tag{E.10}$$

where S_{out} and S_{in} are the output and input power spectral densities (PSD's) of the phase, and B can be shown to be:

$$B^2 = \left(\frac{V_L}{A \cdot V_O}\cos\theta_{ss}\right)^2 = \left(\frac{V_L}{A \cdot V_O}\right)^2 - (\Delta\omega_o)^2. \tag{E.11}$$

If the ILO is being used as a frequency divider, the output phase PSD in (E.10) is divided by N^2, where N is the division ratio [Rat99]. Examining (E.10), it can be seen that the ILO behaves like a first-order phase-locked loop with respect to input phase noise [Rat99], filtering the noise with a low-pass response. Here, the bandwidth of the equivalent low-pass filter is a function of the input injection level.

APPENDIX F
QUALITY FACTOR OF RING OSCILLATOR

It is useful to model the quality factor (Q) of a ring oscillator. This Q can then be applied to the results presented in Appendix E on injection-locked oscillators. Using the model provided in [Ega99], a ring oscillator can be modeled as an ideal inverter with zero delay (providing a 180^o phase shift) in a loop with an element which has a delay of T, as shown in Figure F-1. The delay element causes a phase-shift in the loop equal to

$$\theta = \omega T . \tag{F.1}$$

The loop will oscillate at the frequency where θ is equal to π, since the inverter provides the other 180^o phase shift. Thus, the oscillation frequency is equal to

$$\omega_o = \frac{\pi}{T} . \tag{F.2}$$

The quality factor (Q) of an oscillator is related to the oscillation frequency and phase-shift through the oscillator, as follows [Raz94]:

$$Q = \frac{\omega_o}{2} \cdot \left| \frac{d\theta}{d\omega} \right| . \tag{F.3}$$

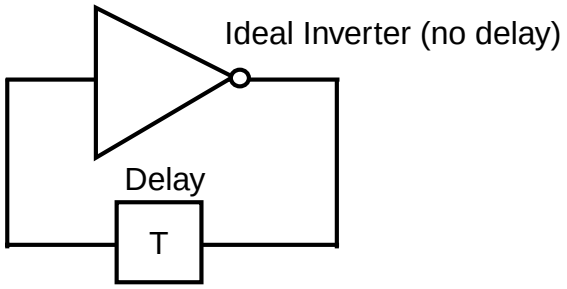


Figure F-1 Model of ring oscillator as an ideal inverter followed by a delay element, used to find the Q of a ring oscillator.

Taking the derivative of (F.1), and applying the result to (F.3) results in [Ega99]

$$Q = \frac{\omega_o}{2} \cdot T = \frac{\pi}{2}. \tag{F.4}$$

Thus, ring oscillators have very low Q's. As a result, they can be injection locked over a very large frequency, since the locking frequency range is inversely dependent on Q, as shown in Appendix E. Also, due to the low Q, ring-oscillators typically have poor phase-noise performance, resulting in higher jitter.

APPENDIX G
RELATIONSHIP BETWEEN JITTER AND PHASE NOISE

The root-mean-squared *phase jitter* is defined as the square root of the variance of the difference between the phase of a signal at the beginning and end of a period, T [Ega99]. This variance is:

$$\sigma_{\phi}^{2} = E\{[\phi(t+T)-\phi(t)]^{2}\}. \tag{G.1}$$

This is converted to jitter in time by simply dividing the phase jitter variance by the square of the angular frequency of the signal. The autocorrelation function of ϕ is

$$R_{\phi}(\tau) = E[\phi(t+\tau)\phi(t)] = \int_{-\infty}^{\infty} L_{\phi}(f)e^{j2\pi f\tau}df, \tag{G.2}$$

where $L_{\phi}(f)$ is the single-sideband phase noise density, and $R(\tau)$ and L(f) are a fourier-transform pair. The single-sideband density is one half the double-sideband phase power spectral density, $S_{\phi}(f)$. Therefore, the jitter variance in time can be expressed as [Haj99]

$$\begin{aligned}
\sigma_{T}^{2} &= \frac{2}{(2\pi f_{o})^{2}}\cdot\left\{\int_{-\infty}^{\infty} L(f)e^{j0}df - \int_{-\infty}^{\infty} L(f)e^{j2\pi fT}df\right\} \qquad \text{(G.3)}\\
&= \frac{2}{(2\pi f_{o})^{2}}\cdot\left\{\int_{0}^{\infty} S_{\phi}(f)df - \frac{1}{2}\int_{0}^{\infty} S_{\phi}(f)e^{j2\pi fT}df - \frac{1}{2}\int_{-\infty}^{0} S_{\phi}(-f)e^{j2\pi fT}df\right\}\\
&= \frac{2}{(2\pi f_{o})^{2}}\cdot\left\{\int_{0}^{\infty} S_{\phi}(f)df - \frac{1}{2}\int_{0}^{\infty} S_{\phi}(f)e^{j2\pi fT}df - \frac{1}{2}\int_{0}^{\infty} S_{\phi}(f)e^{-j2\pi fT}df\right\}\\
&= \frac{2}{(2\pi f_{o})^{2}}\cdot\left\{\int_{0}^{\infty} S_{\phi}(f)[1-\cos(2\pi fT)]df\right\}\\
&= \frac{4}{(2\pi f_{o})^{2}}\cdot\int_{0}^{\infty} S_{\phi}(f)\sin^{2}(\pi fT)df
\end{aligned}$$

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